

*Rambus*

# Rambus Investor Presentation

**R**

Q4 2020



# Safe Harbor for Forward-Looking Statements; Other Disclosures

This presentation contains forward-looking statements under the Private Securities Litigation Reform Act of 1995 including Rambus' financial guidance for future periods, product and investment strategies, timing of expected product launches, demand for existing and newly-acquired technologies, the growth opportunities of the various markets we serve, the expected benefits of our merger, acquisition and divestiture activity, including the success of our integration efforts, and the effects of ASC 606 on reported revenue, amongst other things.

Such forward-looking statements are based on current expectations, estimates and projections, management's beliefs and certain assumptions made by Rambus' management. Actual results may differ materially. Our business is subject to a number of risks which are described more fully in our periodic reports filed with the Securities and Exchange Commission, as well risks and the potential adverse impacts related to, or arising from, the Novel Coronavirus (COVID -19). Rambus undertakes no obligation to update forward-looking statements to reflect events or circumstances after the date hereof.

Effective January 1, 2018, the Company adopted Accounting Standards Update No. 2014-09, Revenue from Contracts with Customers in ASC 606. The adoption of ASC 606 materially impacted the timing of revenue recognition for the Company's fixed-fee intellectual property licensing arrangements. The adoption of ASC 606 did not have a material impact on the Company's other revenue streams, net cash provided by operating activities, or its underlying financial position.


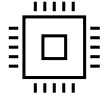
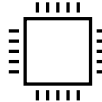
This presentation contains non-GAAP financial measures, including operating costs and expenses, interest and other income (expense), net and diluted net income (loss) per share. In computing these non-GAAP financial measures, stock-based compensation expenses, acquisition-related transaction costs and retention bonus expense, amortization expenses, non-cash interest expense and certain other one-time adjustments were considered. The non-GAAP financial measures should not be considered a substitute for, or superior to, financial measures calculated in accordance with GAAP, and the financial results calculated in accordance with GAAP and reconciliations from these results should be carefully evaluated. Management believes the non-GAAP financial measures are appropriate for both its own assessment of, and to show investors, how the Company's performance compares to other periods. Reconciliation from GAAP to non-GAAP results are made available and more fully described on our website as well as the back of this deck and in the earnings release.

# Rambus at a Glance

## Who We Are

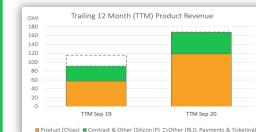
- Premier **silicon IP and chip** provider, making **data faster and safer**
- Developed **foundational technology** for all modern computing systems
- Improving **performance, capacity and security** for leading SoCs and systems

## Rambus Offerings

- Architecture Licenses  High-speed IO & DPA Countermeasures
- Silicon IP  High-speed Interface and Security IP
- Chips  Memory Interface Chips

## Financial Performance

	Q320	2019
Licensing Billings	\$63.1M	\$267.2M
Contract & Other Revenue	\$10.5M	\$60.3M
Product Revenue	\$29.8M	\$73.0M
Cash from Operations	\$44.1M	\$128.5M



NASDAQ:  
RMBS

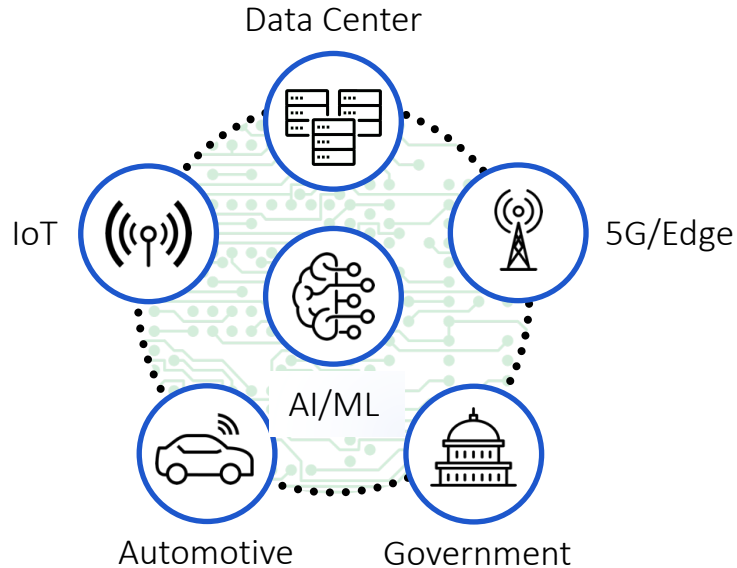
30 Years  
Tech leadership  
& innovation

3000+  
Patents and  
Applications

HQ:  
California  
WW Offices in  
India, EU, Asia

~700  
Employees  
Worldwide

# Data-Intensive Markets Driving Growth



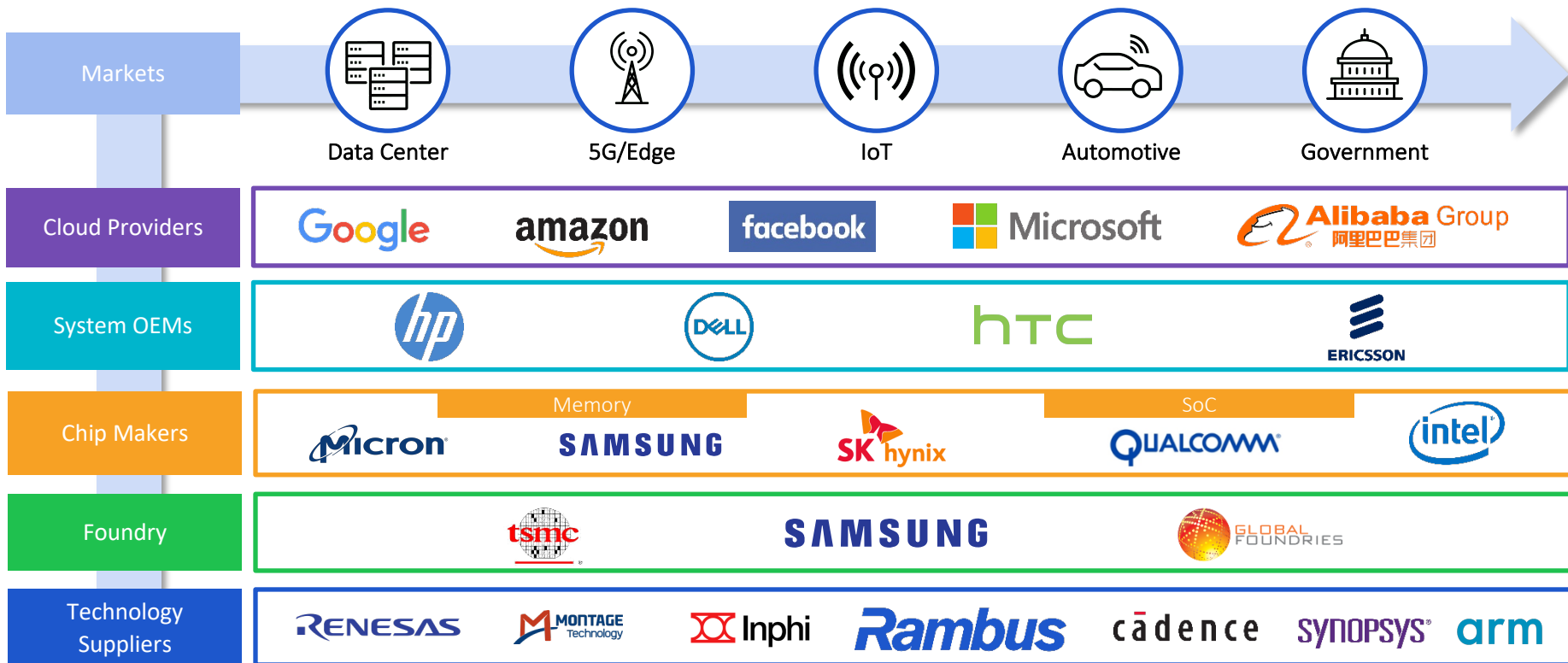
## Global Data Infrastructure Trends

- AI/ML driving up performance requirements across multiple markets
- Platforms shifting to domain-specific systems
- Hyperscalers changing business models and supply chain
- Industry transition to DDR5 progressing
- Complexity and value of data increasing need for security

 Bandwidth & Security 

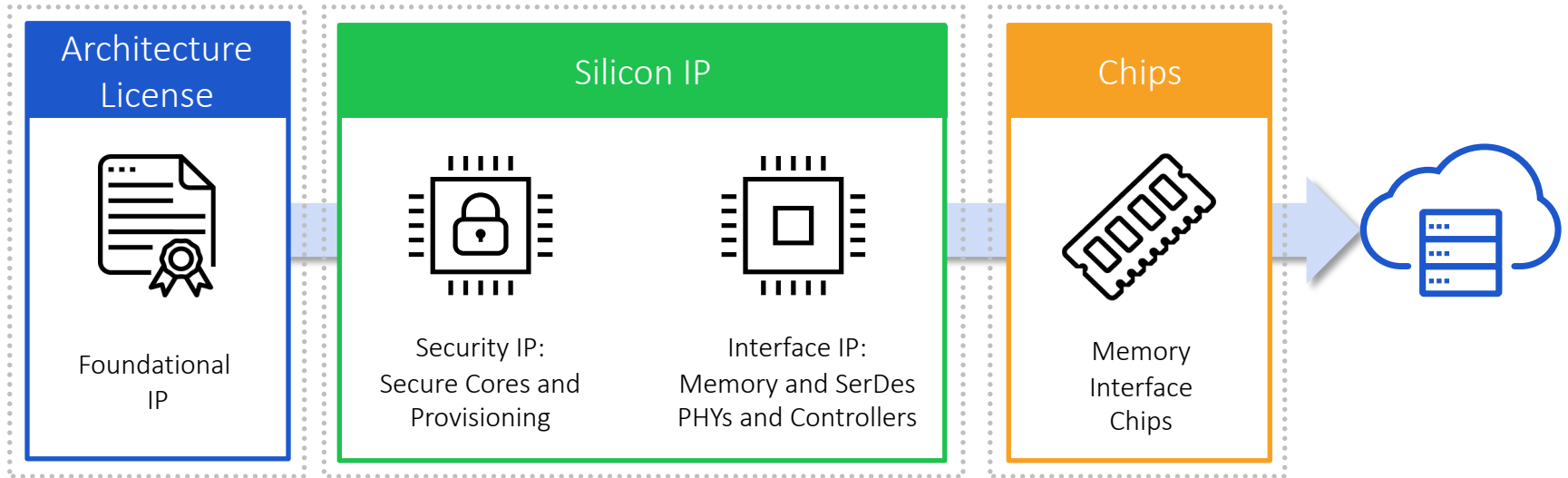


# Semiconductor Industry Ecosystem Built on Leading-Edge IP

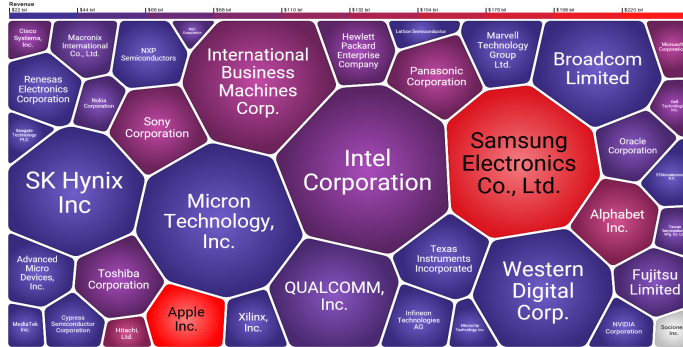
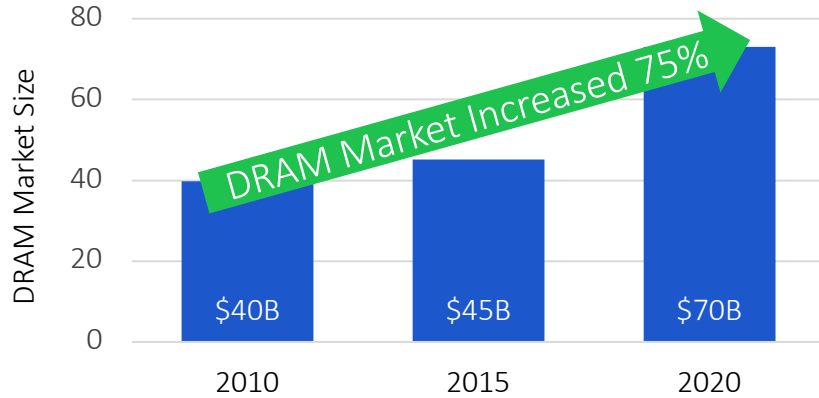


Ecosystem Example

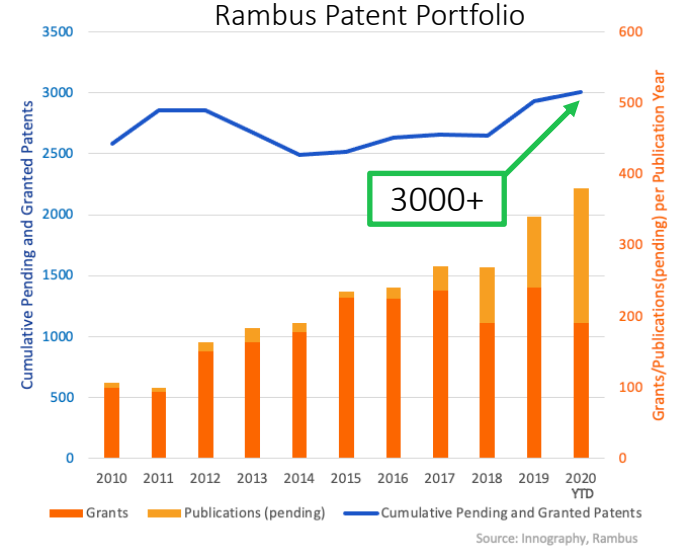
# Semiconductor Solutions Built on Leading-Edge IP



# Strong, Growing and Relevant Patent Portfolio



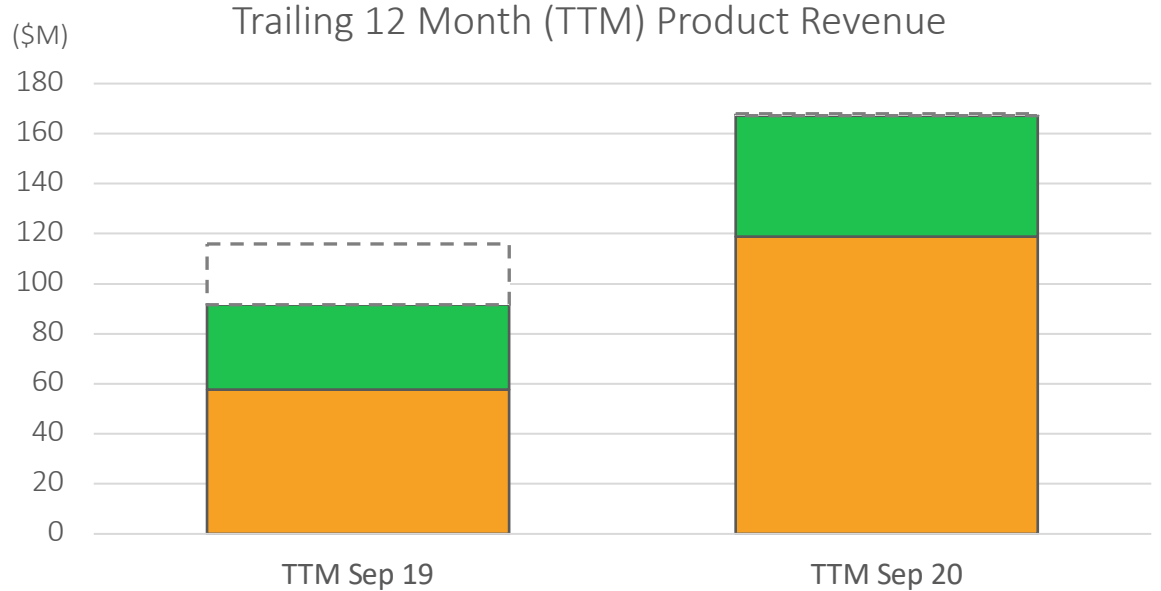
Industry Citations of Rambus Patents



- Growing patent portfolio in key areas:
  - Memory architectures
  - High-speed serial links
  - Embedded security
- Relevant portfolio regularly cited by major industry players

# Products Driving Growth

Increasing momentum in data center, 5G/edge



■ Product (Chips) ■ Contract & Other (Silicon IP) ▨ Other (RLD, Payments & Ticketing)

Contract & Other (~Silicon IP)

\$48.3M TTM Sep '20 revenue  
*up 43%* over TTM Sep '19

Product (~Chips)

\$118.8M TTM Sep '20 revenue  
*doubled* over TTM Sep '19

# Continued Strong Cash Generation

<i>In Millions</i>	<u>ASC 606</u> Q3 2019	<u>ASC 606</u> Q4 2019	<u>ASC 606</u> Q1 2020	<u>ASC 606</u> Q2 2020	<u>ASC 606</u> Q3 2020	
Revenue	\$57.4	\$59.9	\$64.0	\$59.9	\$56.9	Product growth offsets structure and timing of key licensing arrangements.
Total Operating Costs and Expenses <sup>1</sup>	\$67.1	\$62.3	\$63.5	\$59.5	\$56.7	Strong expense management through refocus on core growth initiatives.
Operating Income (Loss) <sup>1</sup>	(\$9.7)	(\$2.3)	\$0.5	\$0.4	\$0.2	Operating results under ASC 606 do not reflect significant cash flow from fixed-fee licensing arrangements
Cash from Operations	\$25.6	\$35.4	\$37.3	\$62.0	\$44.1	Outstanding cash generation

<sup>1</sup>Please refer to reconciliations of non-GAAP financial measures included in this presentation and in our earnings release

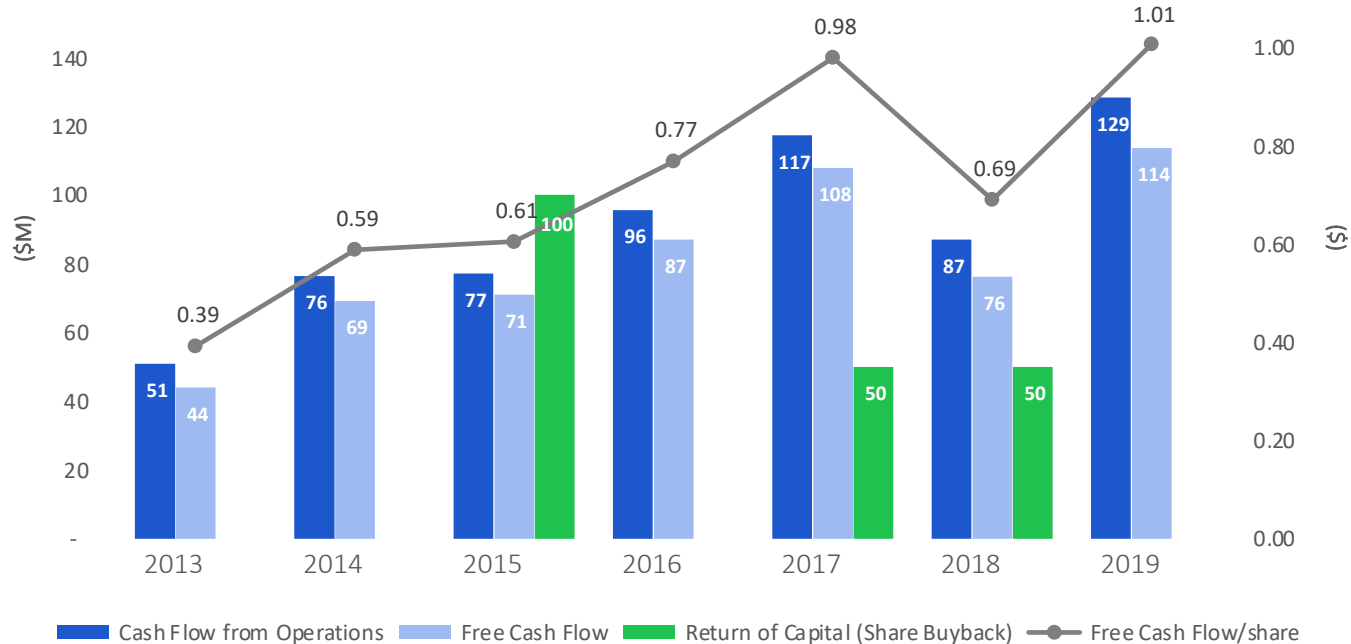
# Solid Balance Sheet Supports Strategic Initiatives

<i>In Millions</i>	Q3 2019	Q4 2019	Q1 2020	Q2 2020	Q3 2020	
Total Cash & Marketable Securities	\$338.0	\$407.7	\$435.4	\$486.1	\$520.2	Provides flexibility to drive strategic initiatives & deliver shareholder value
Total Assets	\$1,299.8	\$1,339.0	\$1,319.5	\$1,316.6	\$1,309.0	Robust balance sheet with limited debt
Stockholders' Equity	\$961.3	\$970.9	\$965.7	\$965.2	\$958.2	\$402M and \$444M contract assets in Q3 2020 and Q2 2020 respectively, related to ASC 606 adoption
Cash from Operations	\$25.6	\$35.4	\$37.3	\$62.0	\$44.1	Outstanding cash generation



# Strong Cash From Operations

Low Capital Expenditure, Consistent Return to Shareholders



- Execution of strategy and operational discipline yields excellent cash flow
- Strong cash position enables flexibility for M&A
- Returned \$200M of cash to shareholders from 2015 through 2018 through Accelerated Share Repurchase programs

# Rambus Investment Summary



Successfully refocused product portfolio around core semiconductor strengths, targeting data center and 5G/Edge



Positioned for long-term profitable growth with predictable licensing base and multiple product revenue streams across company



Continued execution on strategy and strong operational discipline yielding solid financial results



Strong balance sheet and cash generation affords flexibility to drive strategic initiatives



Thank you

**Rambus**  
Data • Faster • Safer

# Reconciliation of Non-GAAP Financial Measures

Net Income (Loss) in Millions	Q3 2019 (ASC 606)	Q4 2019 (ASC 606)	Q1 2020 (ASC 606)	Q2 2020 (ASC 606)	Q3 2020 (ASC 606)
GAAP Net Loss	(\$17)	(\$10)	(\$8)	(\$11)	(\$13)
Adjustments:					
Stock-based compensation	\$7	\$5	\$6	\$7	\$7
Acquisition-related/divestiture costs	\$3	\$4	\$2	\$2	\$1
Amortization	\$3	\$4	\$5	\$5	\$5
Restructuring and other charges	\$1	\$5	\$1	\$0	\$0
Non-cash interest expense	\$2	\$2	\$2	\$2	\$2
Recovery on assets held for sale	(\$2)	(\$8)	\$0	\$0	\$0
Escrow settlement refund	\$0	\$0	\$0	\$0	\$0
Facility restoration costs	\$0	\$1	\$0	\$0	\$0
Change in fair value of earn-out liability	\$0	\$0	(\$2)	\$0	\$0
Provision for (benefit from) income taxes	(\$0)	(\$1)	(\$1)	(\$1)	\$0
<b>Non-GAAP Net Income (Loss)</b>	<b>(\$3)</b>	<b>\$2</b>	<b>\$5</b>	<b>\$3</b>	<b>\$2</b>

Operating Income (Loss) in Millions	Q3 2019 (ASC 606)	Q4 2019 (ASC 606)	Q1 2020 (ASC 606)	Q2 2020 (ASC 606)	Q3 2020 (ASC 606)
GAAP Operating Loss	(\$23)	(\$13)	(\$11)	(\$12)	(\$13)
Adjustments:					
Stock-based compensation	\$7	\$5	\$6	\$7	\$7
Acquisition-related/divestiture costs	\$3	\$4	\$2	\$2	\$1
Amortization	\$3	\$4	\$5	\$5	\$5
Restructuring and other charges	\$1	\$5	\$1	\$0	\$0
Recovery on assets held for sale	(\$2)	(\$8)	\$0	\$0	\$0
Escrow settlement refund	\$0	\$0	\$0	\$0	\$0
Facility restoration costs	\$0	\$1	\$0	\$0	\$0
Change in fair value of earn-out liability	\$0	\$0	(\$2)	\$0	\$0
<b>Non-GAAP Operating Income (Loss)</b>	<b>(\$10)</b>	<b>(\$2)</b>	<b>\$1</b>	<b>\$0</b>	<b>\$0</b>
Depreciation	\$4	\$5	\$5	\$5	\$5
<b>Adjusted EBITDA</b>	<b>(\$5)</b>	<b>\$3</b>	<b>\$5</b>	<b>\$5</b>	<b>\$5</b>

Certain amounts may be off \$1.0M due to rounding.

# Revenue and Licensing Billings

In Thousands	ASC 606					ASC 606			
	Q1'19	Q2'19	Q3'19	Q4'19	FY 2019	Q1'20	Q2'20	Q3'20	Q3'20 YTD
Royalty Revenue	\$24,853	\$27,050	\$19,448	\$19,434	\$90,785	\$19,694	\$16,957	\$16,602	\$53,253
Product Revenue	\$8,964	\$16,031	\$21,377	\$26,600	\$72,972	\$30,728	\$31,725	\$29,769	\$92,222
Contract and Other Revenue	\$14,567	\$15,216	\$16,574	\$13,913	\$60,270	\$13,567	\$11,248	\$10,544	\$35,359
<b>Total</b>	<b>\$48,384</b>	<b>\$58,297</b>	<b>\$57,399</b>	<b>\$59,947</b>	<b>\$224,027</b>	<b>\$63,989</b>	<b>\$59,930</b>	<b>\$56,915</b>	<b>\$180,834</b>

In Thousands	Q1'19	Q2'19	Q3'19	Q4'19	FY 2019	Q1'20	Q2'20	Q3'20	Q3'20 YTD
	Royalty Revenue	\$24,853	\$27,050	\$19,448	\$19,434	\$90,785	\$19,694	\$16,957	\$16,602
Licensing Billings <sup>1</sup>	\$75,460	\$64,948	\$63,058	\$63,758	\$267,224	\$67,072	\$60,687	\$63,135	\$190,894
<b>Delta</b>	<b>\$50,607</b>	<b>\$37,898</b>	<b>\$43,610</b>	<b>\$44,324</b>	<b>\$176,439</b>	<b>\$47,378</b>	<b>\$43,730</b>	<b>\$46,533</b>	<b>\$137,641</b>

In Thousands	Q1'19	Q2'19	Q3'19	Q4'19	FY 2019	Q1'20	Q2'20	Q3'20	Q3'20 YTD
	ASC 606 Interest Income <sup>2</sup>	\$5,707	\$5,288	\$4,925	\$4,469	\$20,389	\$4,368	\$3,697	\$3,289

<sup>1</sup> Licensing billings is an operational metric that reflects amounts invoiced to our patent and technology licensing customers during the period, as adjusted for certain differences.

<sup>2</sup> Interest income associated with the significant financing component of licensing agreements as a result of the adoption of ASC 606.

# GAAP to Non-GAAP Income Statement

In \$ Millions	GAAP Actual Q3'20	Non-GAAP Actual Q3'20	Delta to GAAP
Revenue	\$56.9	\$56.9	\$-
Cost of revenue	15.3	10.9	(4.3)
Research and development	33.7	30.0	(3.7)
Sales, general and administrative	20.4	15.7	(4.7)
Total operating cost and expenses	69.4	56.7	(12.7)
Operating income (loss)	(12.5)	0.2	12.7
Interest and other income (expense), net	0.9	2.7	1.8
Income (loss) before income taxes	(11.6)	2.9	14.5
Provision for income taxes	1.2	0.7	(0.5)
Net income (loss)	(\$12.8)	\$2.2	\$15.0

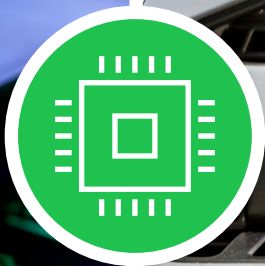
Certain amounts may be off \$0.1M due to rounding.






# Product Overview

**Rambus**  
Data • Faster • Safer



# Silicon IP

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# Silicon IP: Security

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From chip-to-cloud, Rambus secure silicon IP helps protect the world's most valuable resource: data. Securing electronic systems at their hardware foundation, our embedded security solutions span areas including secure co-processors, crypto accelerators, secure protocols, anti-counterfeiting and trusted provisioning.

## Improved Profitability

- Improved time-to-market and reduced inventory waste
- Dynamic SKU and feature management lowers inventory costs
- Reduce revenue lost to unauthorized access and counterfeits

## Superior Security

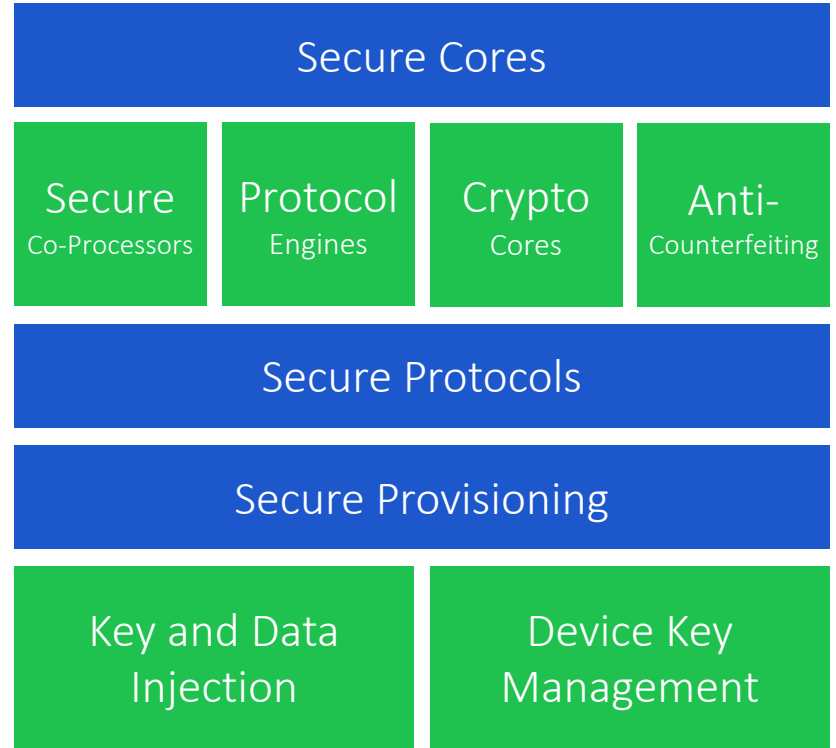
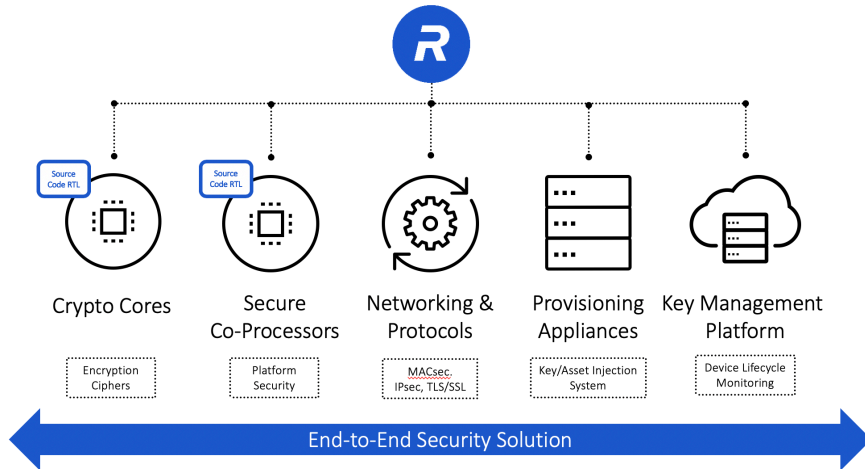
- Provide a robust hardware root-of-trust
- Secure valuable secret keys, identity credentials, intellectual property, and other sensitive data
- Protect against cloning, counterfeiting, and reverse engineering

## Managed Value Chain

- Actively monitor production status, availability, and inventory levels
- Validate process information through secure logs
- Deploy in distributed, high-volume manufacturing

# Silicon IP: Security

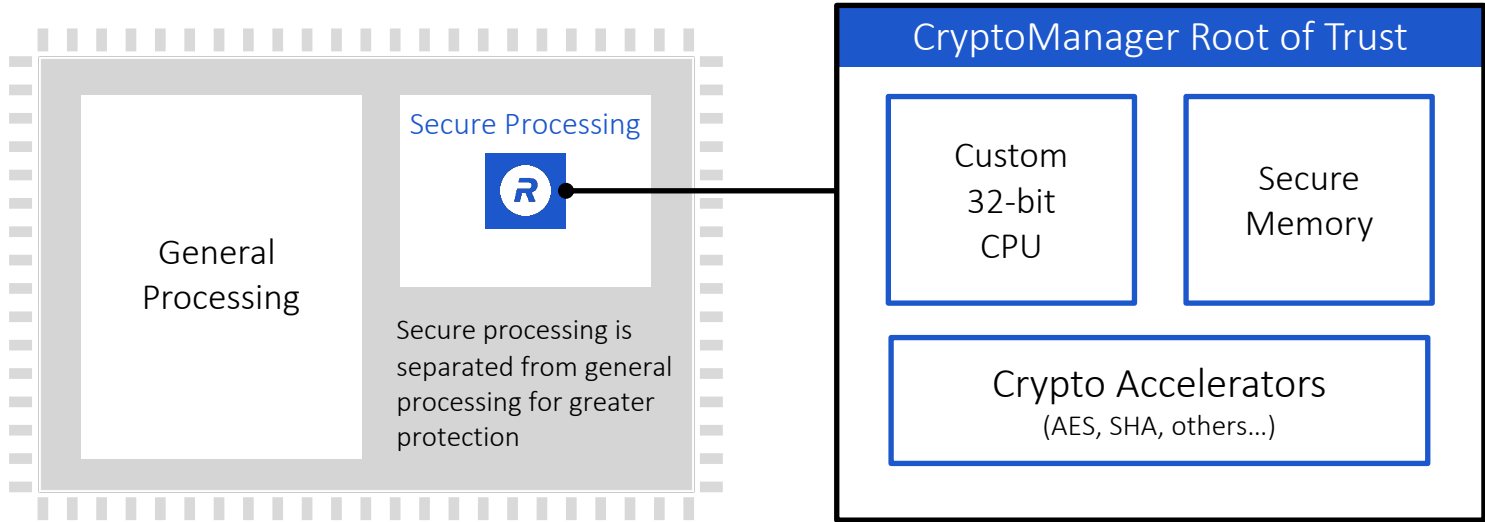
Protecting semiconductors and their secrets from design and manufacturing through deployment and end-of-life



# CryptoManager Root of Trust

Family of fully-programmable secure co-processors

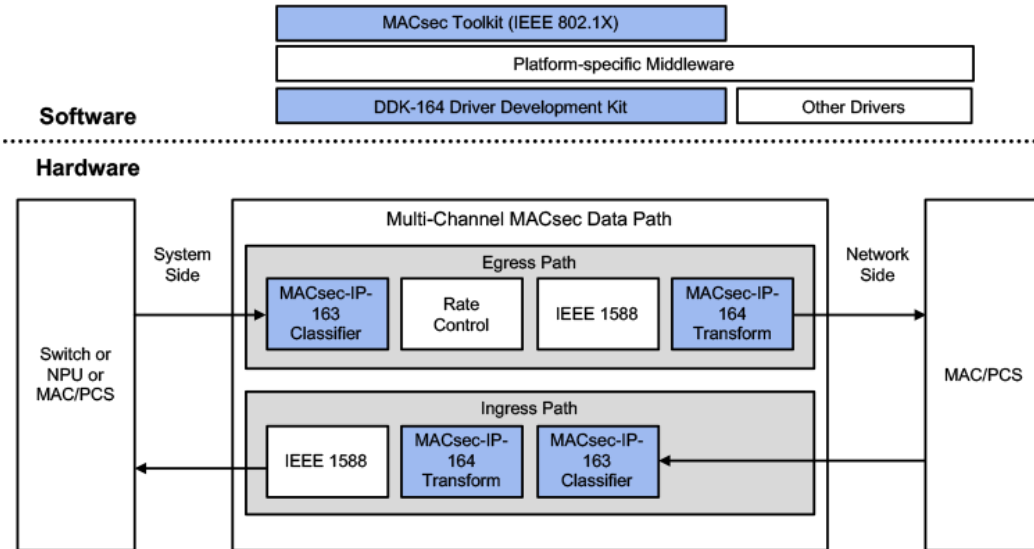
- Protects private data (keys and chip identity) with security anchored in hardware
- Adapts to an evolving threat landscape
- Supports new secure features and applications



Purpose-built for security with defense in depth against attacks

# 800G MACsec Protocol Engine

- Protects data in motion with robust Layer 2 security anchored in hardware
- Operates at full line-rate up to 800 Gbps supporting real-time applications
- Offers easy integration into networking SoCs and ASICs



Multi-channel Protocol Engine Supports 100G to 800G MACsec



# Silicon IP: SerDes PHYs and Controllers

A man in a dark sweater and trousers is walking down a long, brightly lit server aisle. He is holding a laptop. The aisle is lined with server racks on both sides, and the floor has a grid pattern. The lighting is blue and white, creating a modern, high-tech atmosphere.

Optimized for power and area, our line-up of SerDes Interface solutions deliver maximum performance and flexibility for today's most challenging systems.

## Fully Standards-Compatible

- Compliant with the latest industry-standard specifications
- Support for multi-modal functionality

## Enhanced Design Flexibility

- Support for multiple packaging options
- Enhanced margin and yield

## Reduced Power

- Improved power efficiency
- Lower signaling and stand-by power

## Improved Performance

- Increased data rates
- Improved bandwidth
- Higher capacity

# High-Speed SerDes Solutions

## SerDes PHY and digital controller solutions

### 16G

28nm & 14nm

- PCIe 4/3/2
- CEI 11/6
- XFI/XAUI
- SATA
- SAS



### 28G

14nm

- CEI-28/25/11
- 100/10GbE
- FC28
- XFI/XAUI



### PCIe 5

### 32G

7nm

- PCIe 5
- CXL (PHY)
- PCIe 4/3/2

LEAD CUSTOMERS

### 112G

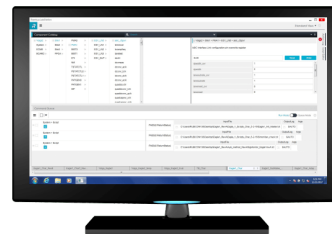
### 56G

7nm

- CEI-112G LR
- CEI-112G XSR
- CEI-56/28/25
- 800/400/200/100GbE
- PAM-4/NRZ

LEAD CUSTOMERS

## Integrated tools for easy bring-up and characterization



LabStation Platform

- Easy-to-use PC Interface
- Interface to 3<sup>rd</sup> party software
- Pre-defined test scripts
- PHY control settings
- External instrument control
- System characteristics and analysis

## Verification tools



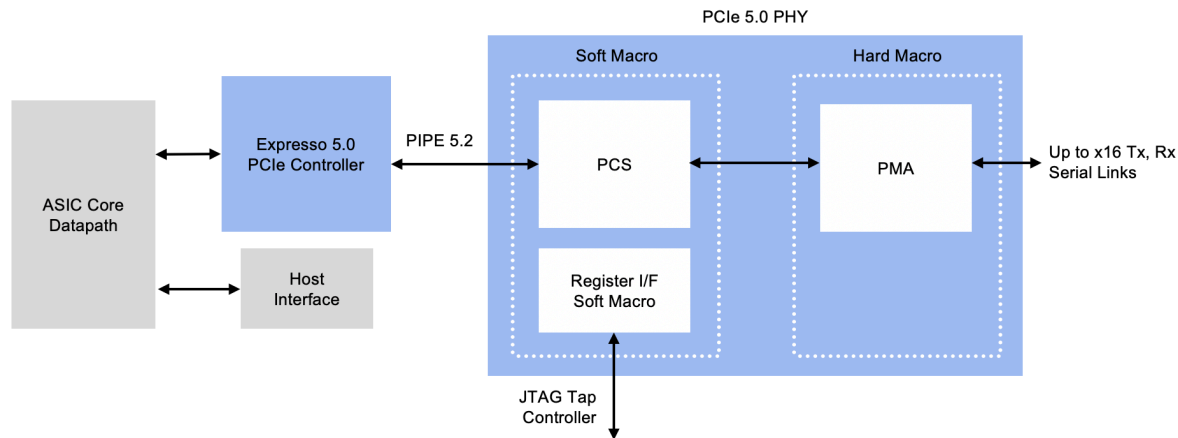
# Complete PCIe 5.0 Interface

## Co-validated PCIe 5 PHY and Controller

- Eases SoC integration effort
- Reduces design risk
- Speeds time to market

## Features

- Backward compatible to PCIe 4/3/2
- PHY supports Compute Express Link (CXL)
- X1, X2, X4, X8 and X16 lane configuration support
- Supports >36dB of channel insertion loss
- Available in 7nm



*PCIe 5 Interface Subsystem*



# Silicon IP: Memory PHYs and Controllers

With their reduced power consumption and industry-leading data rates, our line-up of enhanced memory interface solutions support a broad range of industry standards with improved margin and flexibility.

## Fully Standards-Compatible

- Compliant with the latest JEDEC and industry-standard specifications
- Support for multi-modal functionality

## Enhanced Design Flexibility

- Support for multitude packaging options
- Enhanced margin and yield

## Reduced Power

- Improved power efficiency
- Lower signaling and stand-by power

## Improved Performance

- Increased data rates
- Improved bandwidth
- Higher capacity

# Memory Interface Solutions

## Memory PHY and digital controller solutions

### DDR4/3

28nm & 14nm

- 3200 Mbps
- x16 to x72-bits
- 1-4 Ranks
- DFI 4.0



### HBM2E

7nm

- 3.6 Gbps
- 1024-bit
- 2.5D design architecture



### GDDR6

7nm

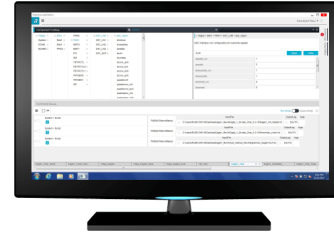
- 12-18 Gbps
- 2x 16-bit channels



### HBM3

ROADMAP

## Integrated tools for easy bring-up and characterization



LabStation Platform

- Easy-to-use PC Interface
- Interface to 3<sup>rd</sup> party software
- Pre-defined test scripts
- PHY control settings
- External instrument control
- System characteristics and analysis

## Verification tools



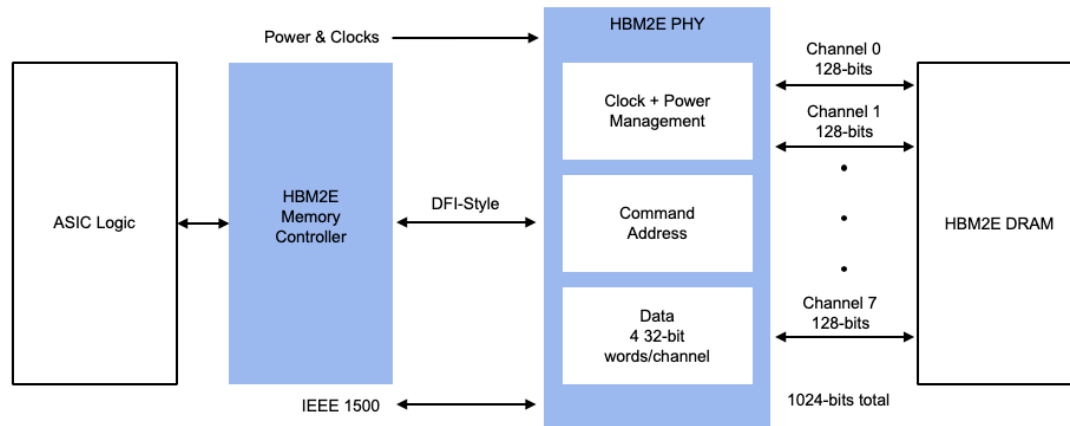
# Complete HBM2E Interface

## Applications

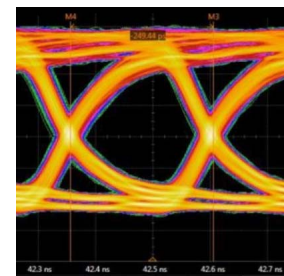
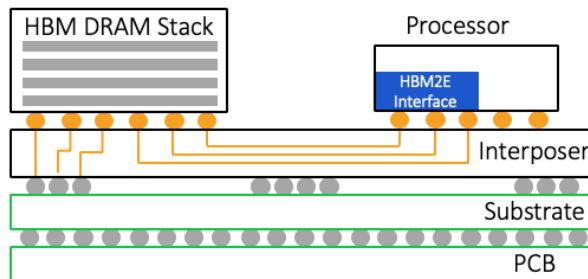
- AI/ML
- Graphics
- Networking

## Features

- JEDEC standard compliant
- 7nm process node
- 461 GB/s maximum bandwidth
- Speed bins to 3.6 Gbps with operation to 4.0 Gbps
- Support for stacks of 2, 4, 8 or 12 DRAM



HBM2E Memory Interface Subsystem  
(Controller & PHY)



World's fastest HBM2E  
Operating at 4.0 Gbps



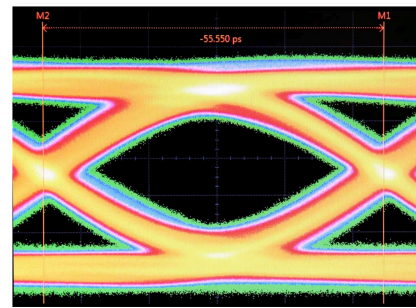
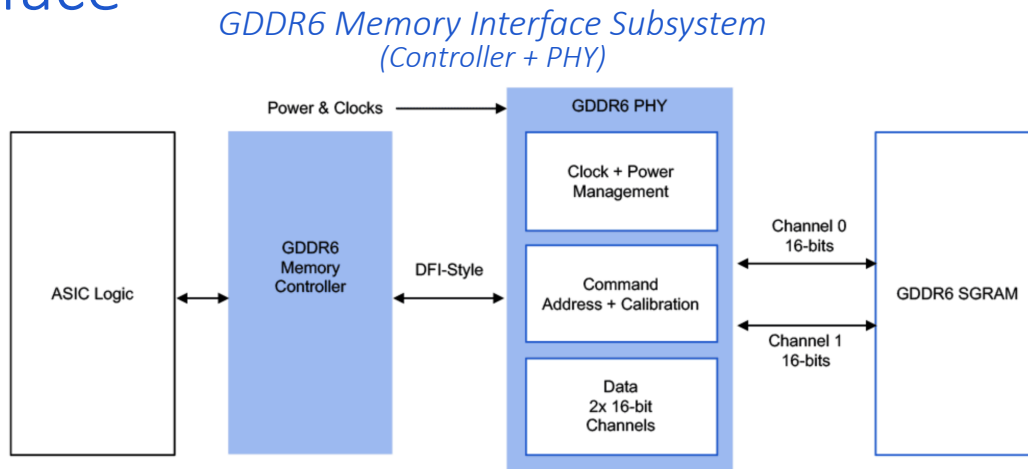
# Complete GDDR6 Interface

## Applications:

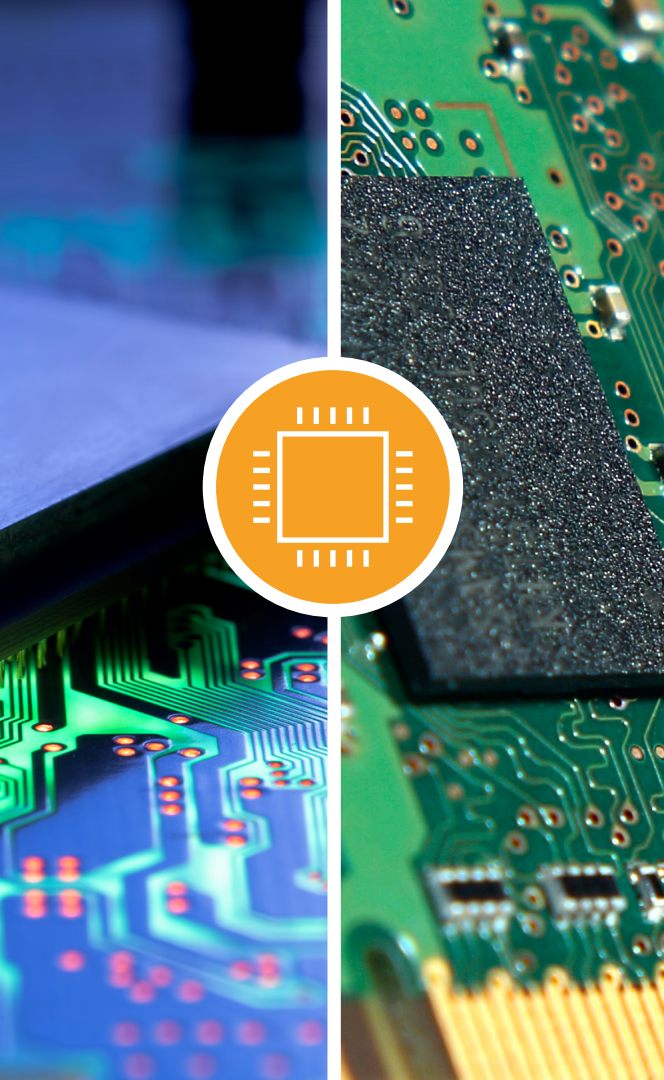
- AI/ML
- Automotive
- Graphics
- Networking

## Features:

- JEDEC standard compliant
- 7nm process node
- 72 GB/s maximum bandwidth
- Speed Bins: 12, 14, 16, 18 Gbps
- Supported DRAM: 8, 12, 16 Gbit
- ASIC Interface: DFI style
- Supports clam shell mode
- All training and calibration modes support



*GDDR6 18 Gbps Transmit Eye*



# Memory Interface Chips

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# Memory Interface Chips

Built for speed, power efficiency and reliability, the DDRn memory interface chips for RDIMM, LRDIMM and NVDIMM server modules deliver top-of-the-line performance and the capacity needed to meet the growing demands on enterprise and data center systems.

## Industry-leading Performance

- Fully-compliant with the latest JEDEC standards
- Operational speeds up to 3200 Mbps

## Enhanced Margin

- Wide margin I/O design with advanced programmability
- Exceed JEDEC reliability standards for ESD and EOS

## Optimized Power

- Advanced power management
- Frequency-based, low-power optimization

## Superior Debug and Serviceability

- Integrated tools for bring-up and debug
- Works out-of-the-box with no BIOS changes required

# Memory Interface Chips

Enabling performance and capacity in server DIMMs

## DDR3

DB & RCD

- JEDEC Compliant
- Speeds up to 2133 Mbps
- Multiple OEM qualifications

AVAILABLE IN PRODUCTION

## DDR4

DB & RCD

- JEDEC Compliant
- Speeds up to 3200 Mbps
- Multiple OEM qualifications

AVAILABLE IN PRODUCTION

## NV

DDR4 NVRCD

- JEDEC Compliant
- Speeds up to 3200 Mbps
- Ongoing qualifications

AVAILABLE IN PRODUCTION

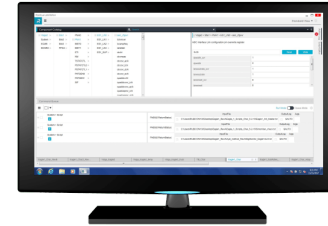
## DDR5

DB & RCD

- Consistent with JEDEC direction

UNDER DEVELOPMENT

Smart tools for easy integration and reduced time to market



LabStation Platform  
and Buffer BIOS Integration Tool

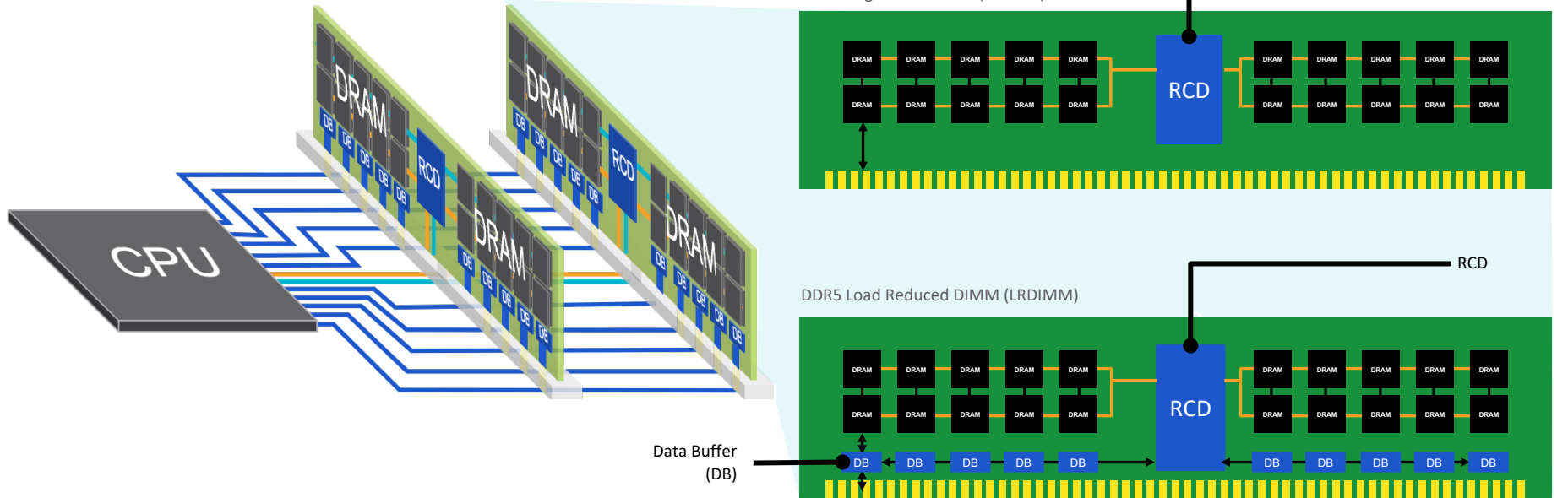
Validated solutions with partners

SAMSUNG



# DDR DIMMs Boost Capacity and Bandwidth

DIMM Memory Interface chips reduce the number of loads to enable higher system capacity and performance



Memory Interface Chips = RCD + DB



Thank you

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