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Rambus, PLDA and Avery Design Announce Comprehensive PCIe 4.0 Solution

Silicon-proven sub-system enables easy integration with pre-validated PHY, controller and verification IP

SUNNYVALE, Calif.--(BUSINESS WIRE)-- [Rambus Inc.](#) (NASDAQ:RMBS), today announced it is collaborating with [PLDA](#), the industry leader in PCI Express[®] controller IP solutions, and [Avery Design Systems Inc.](#), an innovator in functional verification productivity solutions, to offer a comprehensive, silicon-proven PCI Express (PCIe) 4.0 solution, with backward compatibility to PCIe 3.0 and 2.0. The new PCIe sub-system includes a Rambus SerDes PHY, a PLDA PCIe controller and Avery Design's verification IP. The solution is pre-verified and validated for simple integration into application-specific integrated circuits (ASICs).

"Our collaboration with PLDA and Avery Design offers customers a complete, pre-verified PCIe sub-system, with silicon-proven SerDes and a PCIe controller," said Luc Seraphin, senior vice president and general manager of the Rambus Memory and Interfaces Division. "Our line-up of SerDes PHYs is optimized for power and efficiency, delivering maximum performance and flexibility for today's most challenging systems for a variety of applications including networking, data center and high-performance computing."

"Our new solution enables designers to quickly bring their products to market using a sub-system that combines the expertise of proven industry leaders, including Rambus, for their broad portfolio of PHYs, and Avery, for their comprehensive verification solutions," said Arnaud Schleich, CEO at PLDA. "This platform, which supports endpoint, root port and switch applications, demonstrates the high-quality of our PCI Express IP cores, solving performance and integration issues in the market."

"We are excited to team with PLDA and Rambus to offer designers a complete, pre-validated sub-system solution to get their PCIe solution to market," said Chris Browy, vice president of Sales and Marketing at Avery Design. "Pre-qualifying the new PCIe solution with Avery's VIP solutions enables customers to reduce verification cycles and implementation risks for their PCI Express solution."

For additional information on Rambus SerDes PHY, please visit rambus.com/serdes.

Availability

The new PCIe solution is now available worldwide in leading CMOS processes.

For more information, please visit <https://www.rambus.com/memory-and-interfaces/serdes/pcie-phy>.

About Rambus Inc.

Rambus creates innovative hardware and software technologies, driving advancements from the data center to the mobile edge. Our chips, customizable IP cores, architecture licenses, tools, software, services, training and innovations improve the competitive advantage of our customers. We collaborate with the industry, partnering with leading ASIC and SoC designers, foundries, IP developers, EDA companies and validation labs. Our products are integrated into tens of billions of devices and systems, powering and securing diverse applications, including Big Data, Internet of Things (IoT), mobile payments, and smart ticketing. At Rambus, we are makers of better. For more information, visit rambus.com.

About PLDA

PLDA has been successfully delivering PCI and PCI Express IP for 20 years. With over 6,200 licenses, PLDA has established a vast customer base and the world's broadest PCIe ecosystem. PLDA has maintained its leadership over four generations of PCI Express specifications, enabling customers to reduce risk and accelerate time to market for their ASIC and FPGA based designs. PLDA provides a complete PCIe solution with its IP cores, FPGA boards for ASIC prototyping, PCIe BFM/testbench, PCIe drivers and APIs. PLDA is a global company with offices in North America (San Jose, California) and Europe (France, Italy, Bulgaria).

About Avery Design

Founded in 1999, Avery Design Systems, Inc. enables system and SOC design teams to achieve dramatic functional verification productivity improvements through the use of formal analysis applications for RT-level and gate-level X verification; robust core-through-chip-level Verification IP for PCI Express, USB, AMBA, UFS, Unipro, CSI-2/DSI-2, Soundwire, Sensewire, DDR/LPDDR, HBM, HMC, ONFI/Toggle, NVM Express, SAS, SATA, eMMC, SD/SDIO, CAN FD, LIN, FlexRay, HDMI, and DisplayPort standards. The company is a member of the Mentor Graphics Value Added Partnership (VAP) program and has established numerous Avery Design VIP partner program affiliations with leading IP suppliers. More information about the company may be found at www.avery-design.com.

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