Rambus

January 19, 2016

Rambus to Keynote on Silicon Foundations for Security at DesignCon 2016

Additional talks feature technical trainings exploring system design challenges for memory and serial links along with first public demonstration of the R+ 16G Serial Link PHY

SUNNYVALE, Calif.--(BUSINESS WIRE)-- Rambus Inc. (NASDAQ:RMBS)

This Smart News Release features multimedia. View the full release here:
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Who: Â Rambus Inc. (NASDAQ: RMBS)

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Where: DesignCon
         Booth #835
         Santa Clara Convention Center
         5001 Great America Pkwy
         Santa Clara, CA 95054

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When: January 19 - 21, 2016

Join Rambus at DesignCon for the first public demonstration of its R+ 16G Serial Link PHY along with other memory IP core solutions and tools for server, mobile and networking applications. R+ solutions combine innovative technologies and design techniques to offer advanced feature sets and improved functionality while maintaining compatibility with industry standards. Rambus executives and leading engineers will discuss advancements in the design and characterization of high-speed memory and serial link interfaces as well as cryptography and data security for chip architectures.

Rambus Speaking Engagements:

Title: Keynote: Silicon Foundations for Security
Date: Thursday, January 21, 2016
Time: 12:00 pm - 12:45 pm
Topic: The security capabilities and limitations of chips play a critical role in security. Unfortunately, these foundations typically assume complex software will be bug-free. As a result, security failures are increasingly common in today's complex and inter-connected products. Paul Kocher, founder of Cryptography Research, will explore intersections of cryptography and data security with chip architectures. Power analysis attacks will be used as an example of how layers of abstraction can conceal security challenges. The talk will also explore architectures aimed at scaling more securely, including on-chip hardware security solutions for SoCs and infrastructure needs for the manufacturing and management of complex connected devices.
Speaker: Paul Kocher, Chief Scientist, Cryptography Research Division of Rambus Inc.

Title: Analysis, Modeling and Characterization of Multi-Protocol High-Speed Serial Links
Date: Wednesday, January 20, 2016
Time: 9:20 am - 10:00 am
Topic: Improved analysis, modeling, characterization and correlation methods of multi-protocol high-speed transceivers that utilize T-coil to enhance the transmitter and receiver bandwidth, transmitter FIR filters and receiver CTLE and DFE equalizers will be presented. The key circuit blocks are measured and modeled using IBIS-AMI models and the overall system performance including the eye diagrams, BER curves are well correlated to on-die measurements. The paper will also discuss the procedure taken to model, measure and verify the high-speed transceivers to meet the standard specifications such as return loss, jitter tolerance, BER and convergence of the adaptation equalizers and CDR to optimize the margins for various channels.
Speaker: Wendem Beyene, Technical Director, Rambus Inc.

Title: Rethinking System Architectures: The Shifting Performance Bottlenecks Driving Future Silicon Design
Date: Wednesday, January 20, 2016

Time: 9:20 am - 10:00 am and 2:00 pm - 2:40 pm
Topic: Moore's Law has relentlessly delivered tremendous improvements in processing performance and functionality for several decades, enabling newer generations of processors to surpass the capabilities of their predecessors. While processors will continue to become more feature-rich, the emergence of new computing paradigms and slower rates on improvement in other areas mean that power and performance bottlenecks moving away from processors into others subsystems. Moving data between processing elements, memory, storage and across networks is becoming a growing challenge, and concerns about power and security are forcing chip and system architects to rethink not only how silicon needs to be architected, but systems as a whole. In this talk, Rambus discuss how these concerns are driving changes in the way we think about both silicon and systems in the future.
Speaker: Steven Woo, VP, Solutions Marketing and Distinguished Inventor, Rambus Inc.

Title: Which SerDes to Choose: System Tradeoffs For High-speed Serial Link Selection
Date: Wednesday, January 20, 2016
Time: 10:15 am - 10:55 am and 2:50 pm - 3:30 pm
Topic: With the new era of every device getting smart and data getting bigger, there has been a constant increase in bandwidth and speed requirements for networking communications on the back end side. From the age of chips communicating at 1Gbps to 10Gbps to 40Gbps to 100Gbps and setting the stage for 400Gbps and 1Tbps in coming years, everyone wants to communicate faster and faster but at the same time by being more efficient (energy consumption) and smaller (silicon area). With the new technology nodes trending even faster than Moore's law, there are variety of dimensions and tradeoffs which are required to define a Serial link for the next generation needs to make a particular solution effective on all fronts.
Speaker: Mohit Gupta, Director, Product Marketing, Rambus Inc.

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About Rambus Inc.

Rambus creates cutting-edge semiconductor and IP products, spanning memory and interfaces to security, smart sensors and lighting. Our chips, customizable IP cores, architecture licenses, tools, services, training and innovations improve the competitive advantage of our customers. We collaborate with the industry, partnering with leading ASIC and SoC designers, foundries, IP developers, EDA companies and validation labs. Our products are integrated into tens of billions of devices and systems, powering and securing diverse applications, including Big Data, Internet of Things (IoT), mobile, consumer and media platforms. At Rambus, we are makers of better. For more information, visit rambus.com.

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