



October 22, 2015

Rambus to Speak at the Electrical Performance of Electronic Packages and Systems (EPEPS) Conference 2015

SUNNYVALE, Calif.--(BUSINESS WIRE)-- Rambus Inc. (NASDAQ: RMBS):

Who: Rambus Inc. (NASDAQ: RMBS)

Where: EPEPS 2015
DoubleTree by Hilton Hotel San Jose
2050 Gateway Place
San Jose, CA 95110

When: October 25-28, 2015

At [EPEPS 2015](#), the premier international conference on advanced and emerging issues in electrical modeling, analysis and design of electronic interconnections, packages and systems, Rambus executives and leading engineers will discuss advancements in the design and characterization of high-speed memory and serial link interfaces. A detailed agenda of the conference can be found [here](#).

Rambus Speaking Engagements:

Title: Future Challenges for Server Memory in Datacenter and Enterprise Systems

Date: Monday, October 26, 2015

Time: 8:15 - 9 am PT

Topic: Big data and escalating demands on IT are creating an explosion of data and real-time processing requirements that are fueling the need for increased memory speed and capacity across datacenters and enterprise systems. As the industry evolves to meet these needs, there are key challenges in DDR4 memory design that must be addressed. This session will discuss the future fundamental challenges in DDR4 and post-DDR4 that can enable systems to achieve maximum data rates and capacity cost-effectively.

Speaker: Ely Tsern, VP, Chief Technologist, Memory and Interfaces Division, Rambus Inc.

Title: IBIS-AMI Modelling of High-Speed Memory Interfaces (Poster Presentation)

Date: Monday, October 26, 2015

Time: 4:30 - 6 pm PT

Topic: This paper presents techniques to accelerate the exploration of advanced memory links through IBIS-AMI modelling of the transmitter and receiver. The results show over 1000x CPU time speed improvement compared to full transistor level SPICE simulations while providing a fair representation of the interface performance. To demonstrate the versatility the IBIS-AMI for memory interfaces, data transmission at 2.4 Gbps and 6.4 Gbps, over the same multidrop channel with different equalization features, are presented.

Speakers: Arash Zargaran-Yazd and John Yan, Signal Integrity Engineers, Rambus Inc.

Title: Voltage and Time Margin Analysis for Wireline Links in High Dimensional Design Spaces

Date: Wednesday, October 28, 2015

Time: 9 - 10 am PT

Topic: Evaluating the time and voltage margin (vtMargin) of a wireline link across all possible corner cases is deemed unfeasible using time-domain methods. Statistical methods provide estimates at a fraction of time, at the potential cost of accuracy and neglecting the nonlinear behaviors of various link elements. We present a methodology to calculate the vtMargin of memory and serial links in a time-efficient manner while considering nonlinear behaviors of active blocks. Using a small initial dataset, regression analysis is performed to find multi-variable multi-order equations, which are then exhaustively evaluated across all possible combinations of corner cases to find a more comprehensive histogram representing the margin spread in the link.

Speakers: Arash Zargaran-Yazd and John Yan, Signal Integrity Engineers, Rambus Inc.

Title: Return Loss Characterization and Analysis of High-Speed Serial Interface

Date: Wednesday, October 28, 2015

Time: 9 - 10 am PT

Topic: This paper describes the return loss characterization and analysis of a high-speed serial interface with T-coils at the transmitter and receiver. Today's high-speed links utilize equalization to mitigate channel loss and dispersion. In addition, T-coil networks are used at inputs and outputs to improve impedance matching and to enhance the receiver and transmitter bandwidth. To guarantee the transceiver performance, a wide range of Serializer Deserializer (SerDes) compliance specifications exist for the return loss measured at or near the package interface and the Printed Circuit Board (PCB). For multi-protocol SerDes, thus, T-coil networks are often necessary to meet the most stringent return loss specification. This paper presents the analysis and characterization of a high-speed transceiver with T-coils designed in a 28 nm CMOS process. Measurements are also presented to demonstrate the improvement in return loss and bandwidth of the transceiver.

Speakers: Chris Madden, Senior Principal Engineer, Wendem Beyene, Technical Director, Hai Lan, Senior Manager, Signal Integrity Engineering, Rambus Inc., and Nikhil Vaidya, Circuit Design Engineer, Rambus Inc.

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About Rambus Memory and Interfaces Division (MID)

The Rambus Memory and Interfaces Division develops products and services that solve the power, performance, and capacity challenges of the mobile, connected device, and cloud computing markets. Rambus enhanced standards-compatible and custom memory and serial link solutions include chips, architectures, memory and chip-to-chip interfaces, DRAM, IP validation tools, and system and IC design services. Developed through our system-aware design methodology, Rambus products deliver improved time-to-market and first-time-right quality.

About Rambus Inc.

Rambus creates cutting-edge semiconductor and IP products, spanning memory and interfaces to security, smart sensors and lighting. Our chips, customizable IP cores, architecture licenses, tools, services, training and innovations improve the competitive advantage of our customers. We collaborate with the industry, partnering with leading ASIC and SoC designers, foundries, IP developers, EDA companies and validation labs. Our products are integrated into tens of billions of devices and systems, powering and securing diverse applications, including Big Data, Internet of Things (IoT), mobile, consumer and media platforms. At Rambus, we are makers of better. For more information, visit rambus.com.

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