January 28, 2014

Rambus Engineers and Scientists to Present New Research and Training at DesignCon 2014

SANTA CLARA, Calif.--(BUSINESS WIRE)-- Rambus Inc. (NASDAQ:RMBS):

Who: Rambus Inc. (NASDAQ:RMBS)

Where: DesignCon
Santa Clara Convention Center - Booth #301
5001 Great America Parkway, Santa Clara, Calif.
DesignCon.com

When: January 28 - 31, 2014

At DesignCon 2014, Rambus engineers and scientists will present two papers on the latest research in ultra-high speed interface design and deliver training on the latest low-power, high-performance memory solutions.

Additionally, Rambus will be demonstrating various IP cores, tools and emerging architectures designed to deliver robust and easy to integrate solutions in its booth (#301), including: the LabStation™ validation platform, R+™ LPDDR3, and R+ technologies for extending main memory beyond DDR4.

Click to Tweet: @rambusinc will be exhibiting, speaking and demonstrating at @UBMDesignCon 2014 on 1/28-31 #Innovation

Paper Presentations:

Title: "An Implementer's Guide to Low-Power and High-Performance Memory Solutions"
Rambus Speakers/Authors: Scott Best, Wendem Beyene, Ming Li
Date: Tuesday, January 28, 2014
Time: 9:00 a.m.-12:00 p.m.

This session provides an in-depth analysis of standard DRAM memory solutions for low-power and high-performance applications. Specifically, the session will cover the interactions between signaling, clocking and packaging technology of a memory interface, and how this knowledge can be used to analyze and compare different popular memory interfaces for different applications including mobile, compute, graphics, and server.

Title: "Lessons Learned: How to Make Predictable PCB Interconnects for Data Rates of 50 Gbps and Beyond"
Rambus Speakers/Authors: Wendem Beyene
Date: Wednesday, January 29, 2014
Time: 9:20 a.m.-10:00 a.m.

Rambus joins colleagues from the industry to discuss elements for 50 Gbps interconnect design success. The discussion will address practical methodology for dielectric and conductor roughness model identification for accurate analysis of 50 Gbps interconnects, understanding the importance of loss separation in conductor roughness and dielectric models, and the impact of fiber weave effects on signal propagation at higher frequencies.

Title: "Package-PCB Interface Discontinuity Optimization for 50 GB/S SerDes Applications"
Rambus Speakers/Authors: Wendem Beyene, Kevin Cai, Gnanadeep Kollipara, Keisuke Saito
Date: Wednesday, January 29, 2014
Time: 11:05 a.m.-11:45 a.m.

This session is focused on system design optimization techniques for the package-PCB interface of a 50Gb/s medium-reach SerDes channel. A summary of optimized design features and relative performance results are presented for conventional and

high-density interconnect (HDI) PCB designs.

About Rambus Memory and Interfaces Division (MID)

The Rambus Memory and Interfaces Division moves data. MID develops products and services that solve the power, performance, and capacity challenges of the mobile, cloud computing and connected device markets. Rambus enhanced standards-compatible and custom memory and serial link solutions include architectures, memory and chip-to-chip interfaces, DRAM, IP validation tools, and system and IC design services. Developed through our system-aware design methodology, Rambus' products deliver improved time-to-market and first-time-right quality.

About Rambus

Rambus brings invention to market. Our customizable IP cores, architecture licenses, tools, services, and training improve the competitive advantage of our customers' products while accelerating their time-to-market. Rambus products and innovations capture, secure and move data. For more information, visit rambus.com.

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