Rambus and Denali to Provide Complete DDR Memory Controller Design Solutions

Enables Integration of Physical and Logic Layers, Reducing Risk and Improving Time to Market for Memory System Makers

WESTFORD, Mass.--May 13, 2004-- Rambus Inc. (Nasdaq:RMBS), a leading developer of chip interface products and services, and Denali Software, a leading provider of semiconductor intellectual property (IP) and electronic design automation (EDA) tools for chip interface design and verification, today announced plans to jointly provide DDR memory controller design solutions. Combining Rambus drop-in DDR interface cells with Denali's Databahn DDR controller IP provides chip designers with an integrated design environment that will reduce risk and improve time to market when developing and verifying DDR memory controller interfaces.

"Increasing memory speeds and new memory architectures are only two of the critical issues engineers have to worry about when designing a memory system," said Rich Warmke, director of marketing of the Memory Interface Division at Rambus. "Denali has generated significant momentum in the DDR controller space and partnering with them allows us to provide our customers with proven, configurable solutions that make it easier for engineers to develop high-performance memory systems."

Denali memory controllers and Rambus DDR1/DDR2 interface cells easily integrate together into complete memory solutions on customers' designs. Rambus is providing a new family of DDR memory controller interfaces, including mainstream DDR1 and DDR2 up to 800MHz data rates and graphics DDR, including GDDR1, GDDR2, and GDDR3 up to 1600MHz data rates. Rambus DDR memory controller interface cells are full-featured drop-in physical layer (PHY) cells. The interface cells use proven technology that allow customers to dramatically improve time to market, minimize design risk and avoid potential re-spin costs. Rambus also offers system engineering services to further accelerate time to market, and ensure the interface operates at high frequency in the system environment. The solution is additionally supported with Denali's verification IP products for simulating and verifying the memory system before implementation in silicon.

"We're pleased to be able to help our customers reduce risk and overall development time through our alliance with Rambus," said Mike McKeon, director of strategic products at Denali. "Denali's silicon-proven Databahn controllers, combined with Rambus's interface cells, is ideal for customers who need maximum speed and reliability, and minimum design risk for their memory interfaces."

Details of the joint DDR memory system solution will be presented at the MemCon event starting today in Westford, Massachusetts. The full-day event is focused on DDR2 systems and technology, and features exclusive presentations from Denali, Rambus, and 9 other memory companies. Registration is free to industry professionals online at: http://www.memcon.com.

Additional information about the Rambus family of DDR memory controller interfaces can be found online at www.rambus.com/products/ddr. More information about Denali's Databahn memory controllers and memory verification IP can be accessed on Denali's Web site at http://www.denali.com.

About Rambus Inc.

Rambus is one of the world's leading providers of advanced chip-to-chip interface products and services. Since its founding in 1990, the company's innovations, breakthrough technologies and integration expertise have helped industry-leading chip and system companies solve their most challenging and complex I/O problems and bring their products to market. Rambus's interface solutions can be found in numerous computing, consumer, and communications products and applications. Rambus is headquartered in Los Altos, Calif., with regional offices in the United States, Taiwan and Japan. Additional information is available at www.rambus.com.

About Denali Software, Inc.

Denali Software Inc. is the world's leading provider of electronic design automation (EDA) software and Semiconductor Intellectual Property (SIP) solutions for chip interface design, integration, and verification. More than 400 companies worldwide use Denali's tools, technology, and services to design and verify complex chip interfaces for communication, consumer, and computer products. Corporate headquarters are located at: 1850B Embarcadero Road, Palo Alto, Calif. 94303. For more information, visit Denali at www.denali.com. Or, contact Denali by phone at (650) 461-7200, or email info@denali.com.

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This release contains forward-looking statements that are made pursuant to the safe harbor provisions of the Private Securities Litigation Reform Act of 1995. Forward-looking statements include statements about customers' abilities to improve time to market, minimize design risk, improve performance, and lower costs, including avoiding potential re-spin costs. Forward-looking statements further include suitability and availability for computing, consumer and communications markets, as well as the dates of when DDR-based interfaces are expected to be available in the respective markets. Additional forward-looking statements include the ability of Rambus DDR interface cells to provide design flexibility in silicon proven process technologies. These forward-looking statements are subject to risks and uncertainties, which could cause actual results to differ materially from those projected. Those risks include the possibility of technical problems with the interface cells that reduce or eliminate time to market, design risk minimization, performance or cost benefits, reduced market adoption of the DDR interface cells, negative market response to these products, any delay in the development of Rambus-based products by licensees, any delay in the development and shipment of new Rambus products, any delay in the development and shipment of products compatible with Rambus products, a strong response of the market to competing technology, a failure to sign new contracts or maintain existing contracts for DDR cell technologies, adverse litigation decisions and other factors that are described in our SEC filings including our 10-K and 10-Qs

Note to Press: Rambus announced the availability of its broad family of DDR memory controller interface cells and service on May 10, 2004. For more information, please refer to the press release at www.rambus.com/news/pressreleaselist.cfm.

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