Rambus Provides DDR and GDDR Memory Controller Interface Cells and Services; Expands Product Offering to Become One-Stop Shop for Memory Interfaces

LOS ALTOS, Calif.--May 10, 2004--Rambus Inc. (Nasdaq:RMBS), a leading developer of chip interface products and services, today announced the availability of a broad family of double data rate (DDR) memory controller interface cells and services. Providing support for mainstream DDR1 and DDR2 up to 800MHz data rates and graphics DDR, including GDDR1, GDDR2, and GDDR3 up to 1600MHz data rates, Rambus DDR memory controller interface cells are full-featured drop-in physical layer (PHY) cells. The interface cells use proven technology that allow customers to dramatically improve time to market, minimize design risk and avoid potential re-spin costs. Rambus also offers system engineering services to further accelerate time to market, and ensure the interface operates at high frequency in the system environment. Rambus DDR interface solutions are ideal for a broad range of applications, from consumer multimedia and graphics systems to mainstream PCs and servers.

"As DDR memory interfaces become faster and as a result more challenging to design, a growing number of customers are requesting proven solutions," said Laura Stark, vice president of the Memory Interface Division at Rambus. "By using Rambus DDR solutions for the memory interface, chip designers can focus on other critical portions of the chip. This new solution, along with RDRAM® and XDR™ memory interfaces, rounds out our product portfolio and provides a memory interface for any level performance need."

Rambus DDR memory controller interfaces are complete interface cells instead of technology building blocks, such as I/O pads and delay lock loops (DLLs) that engineers must assemble, integrate and verify on their own. By incorporating Rambus's drop-in DDR memory controller interface cells into their chip designs, customers can save an estimated six-to-nine months of development time and potentially millions of dollars by avoiding costly chip re-spins and lost revenues from being late to market. As with all Rambus interface solutions, Rambus DDR interface cells are designed to integrate seamlessly into silicon, and provide improved time-to-market, lower design risk, higher performance, and lower total cost.

Additionally, Rambus is the only company to provide DDR memory controller interfaces with an optional performance mode supporting XDR DRAM, enabling a two-to-eight times increase in system memory bandwidth. Using this capability, customers can develop a single chip that spans multiple price/performance points depending on which memory type is connected.

Rambus DDR interface circuits are designed for a wide variety of standard CMOS processes, such as 90 nanometer, 0.13-micron and 0.18-micron, and are available immediately on the TSMC 0.13-micron process. Rambus DDR memory controller interfaces for consumer and graphics applications are available now, and those for main memory applications will be available soon.

Rambus will host a web seminar on May 20, 2004 at 10:00 a.m. PDT to outline its DDR interface cells and services. Register at www.rambus.com/news/events. Additional information about the Rambus family of DDR memory controller interfaces can be found at www.rambus.com/products/ddr.

About Rambus Inc.

Rambus is one of the world's leading providers of advanced chip interface products and services. Since its founding in 1990, the company's innovations, breakthrough technologies and integration expertise have helped industry-leading chip and system companies solve their most challenging and complex I/O problems and bring their products to market. Rambus's interface solutions can be found in numerous computing, consumer, and communications products and applications. Rambus is headquartered in Los Altos, Calif., with regional offices in the United States, Taiwan and Japan. Additional information is available at www.rambus.com.

This release contains forward-looking statements that are made pursuant to the safe harbor provisions of the Private Securities Litigation Reform Act of 1995. Forward-looking statements include statements about customers' abilities to improve time to market, minimize design risk, improve performance, and lower costs, including avoiding potential re-spin costs. Forward-looking statements further include suitability and availability for computing, consumer and communications markets, as well as the dates of when DDR-based interfaces are expected to be available in the respective markets. Additional forward-looking statements include the ability of Rambus DDR interface cells to provide design flexibility in silicon proven process technologies. These forward-looking statements are subject to risks and uncertainties, which could cause actual results to differ materially from those projected. Those risks include the possibility of technical problems with the interface cells that reduce or eliminate time to market, design risk minimization, performance or cost benefits, reduced market adoption of the DDR interface cells, negative market response to these products, any delay in the development of Rambus-based products by licensees, any delay in the development and shipment of new Rambus products, any delay in the development and shipment of products compatible

with Rambus products, a strong response of the market to competing technology, a failure to sign new contracts or maintain existing contracts for DDR cell technologies, adverse litigation decisions and other factors that are described in our SEC filings including our 10-K and 10-Qs.

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