Rambus

Rambus Investor Presentation

Q2 2021

Safe Harbor for Forward-Looking Statements; Other Disclosures

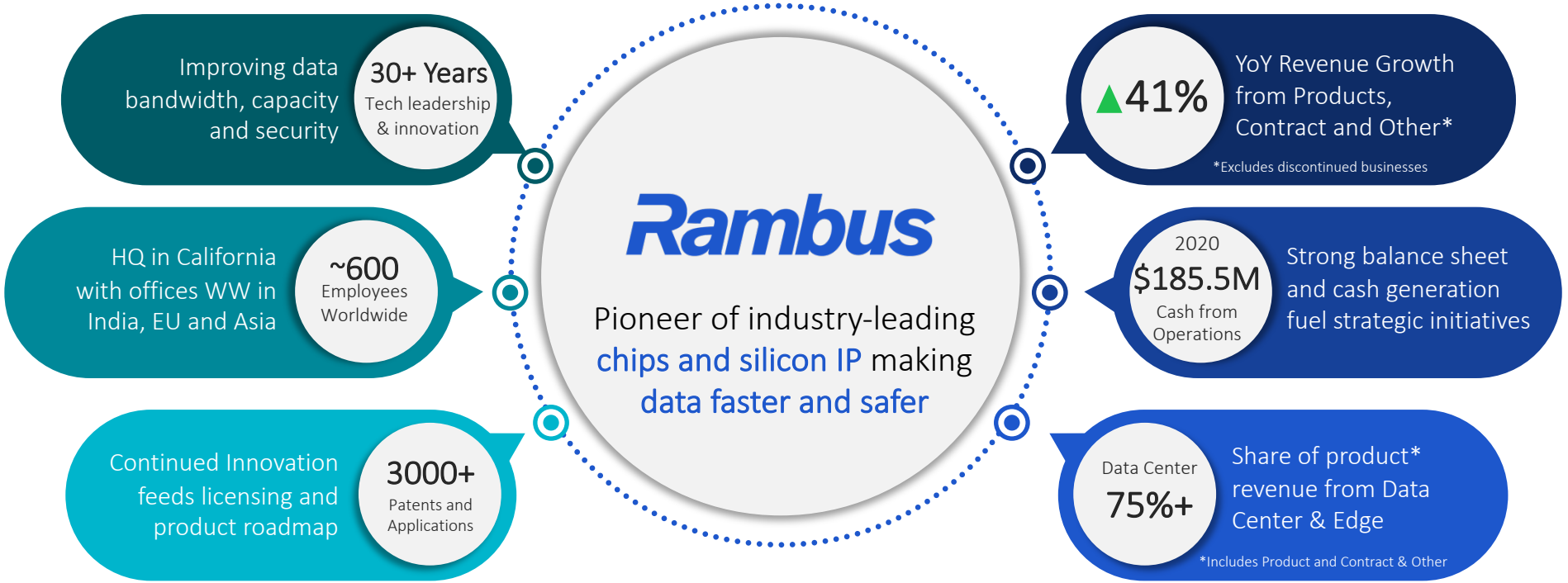
This presentation contains forward-looking statements under the Private Securities Litigation Reform Act of 1995, including those relating to drivers of the Company's topline growth; the Company's ability to deliver ongoing profitable growth; the Company's outlook for the second quarter of 2021; the Company's strategic opportunities and initiatives as well as related outcomes; and the expected terms, timing, completion and effects of the acquisitions of PLDA and AnalogX.

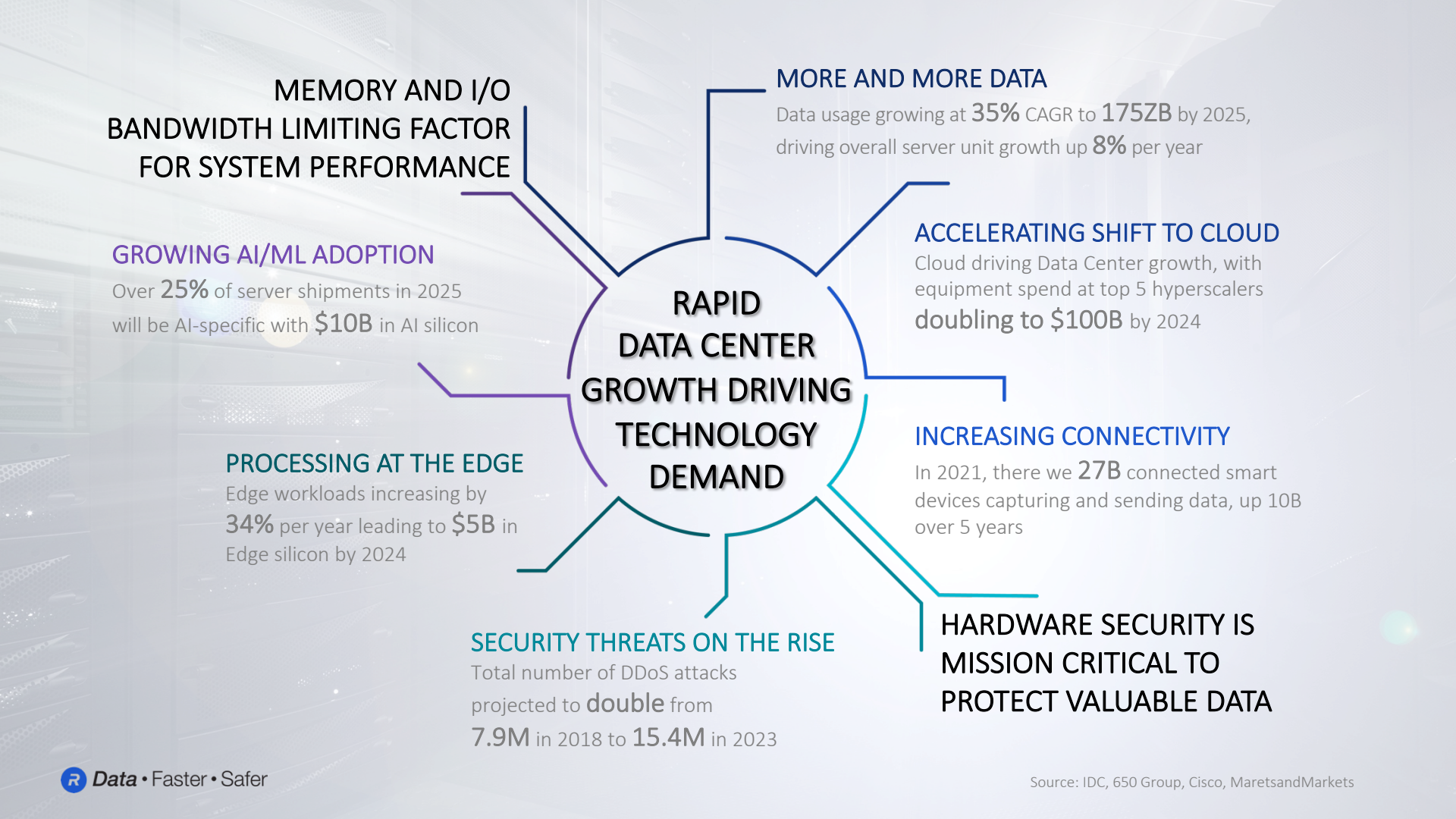
Such forward-looking statements are based on management's current expectations, assumptions, beliefs, estimates and projections. Actual results may differ materially. The Company's business generally and forward-looking statements in this presentation are subject to a number of risks that are more fully described in Rambus' Annual Report on Form 10-K and Quarterly Reports filed on Form 10-Q, as filed with the Securities and Exchange Commission. The Company undertakes no obligation to update forward-looking statements to reflect events or circumstances after the date hereof, except as required by law.

Effective January 1, 2018, the Company adopted Accounting Standards Update No. 2014-09, Revenue from Contracts with Customers in ASC 606. The adoption of ASC 606 materially impacted the timing of revenue recognition for the Company's fixed-fee intellectual property licensing arrangements. The adoption of ASC 606 did not have a material impact on the Company's other revenue streams, net cash provided by operating activities, or its underlying financial position.

This presentation contains non-GAAP financial measures, including operating costs and expenses, interest and other income (expense), net and diluted net income (loss) per share. In computing these non-GAAP financial measures, stock-based compensation expenses, acquisition-related transaction costs and retention bonus expense, amortization expenses, depreciation expense on unused Electronic Design Automation ("EDA") software licenses, expense on abandoned operating leases, restatement and shareholder activist costs, non-cash interest expense and certain other one-time adjustments were considered. These non-GAAP financial measures should not be considered a substitute for, or superior to, financial measures calculated in accordance with GAAP. You should carefully review the reconciliation of each non-GAAP financial measure to the most comparable GAAP measure, as set forth in the appendix hereto. Management believes that the non-GAAP financial measures contained herein are helpful to investors in allowing for an assessment of the Company's performance period over period.

Rambus at a Glance

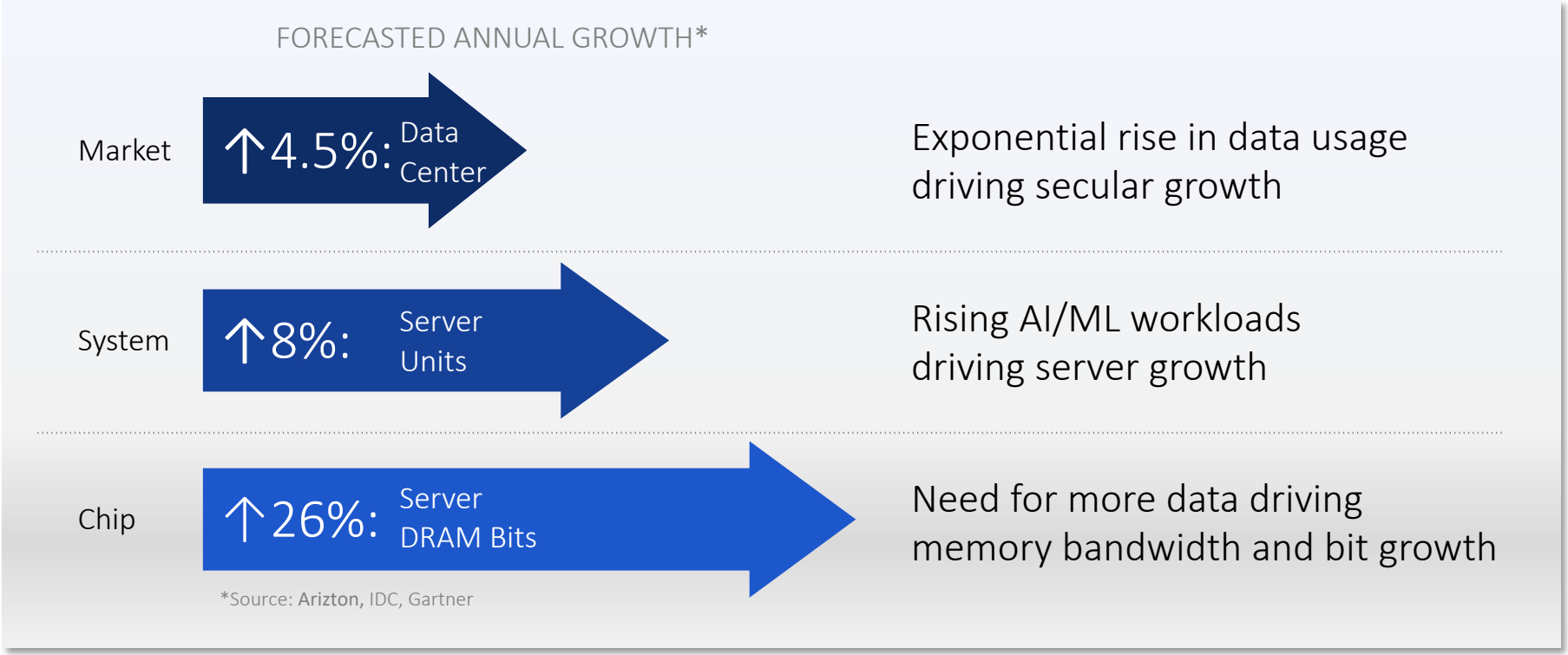




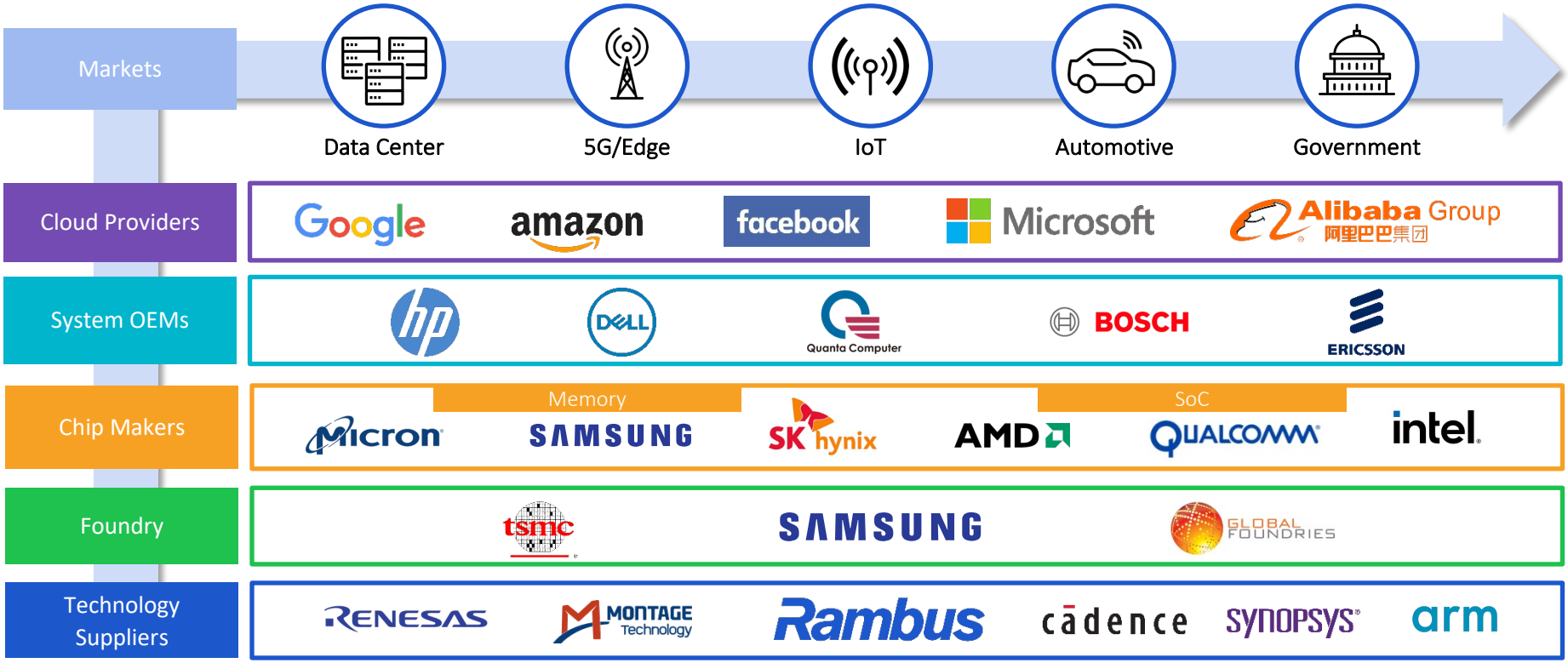
Source: IDC, 650 Group, Cisco, MaretsandMarkets

Amplified Market Opportunity

Increasing need for bandwidth and security



Semiconductor Industry Ecosystem Built on Leading-Edge IP



Ecosystem Example

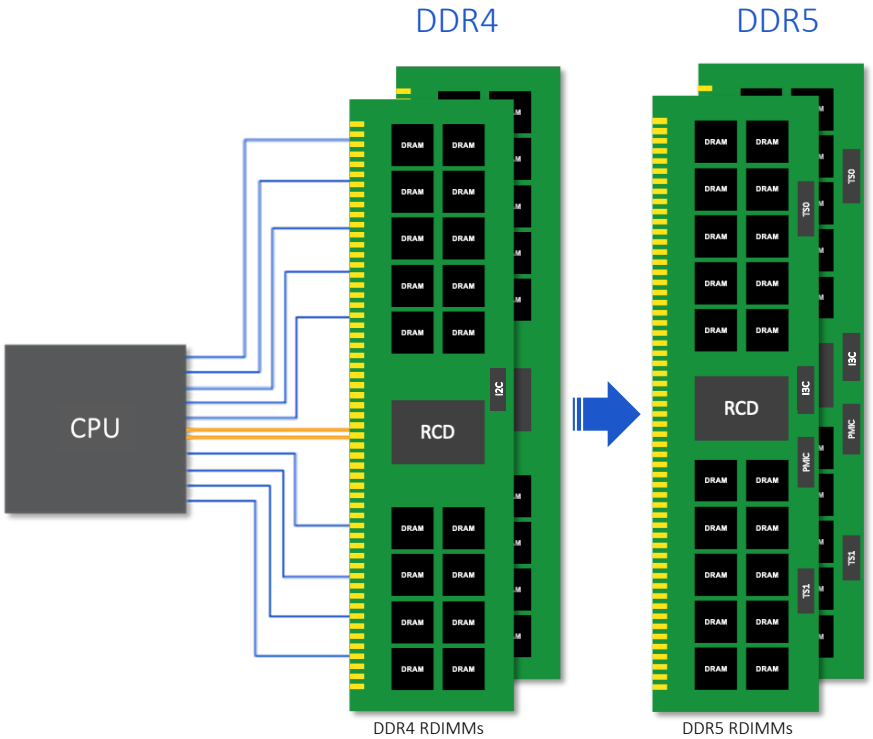
Rambus Memory Interface Chip Growth

2018-2020

72% CAGR

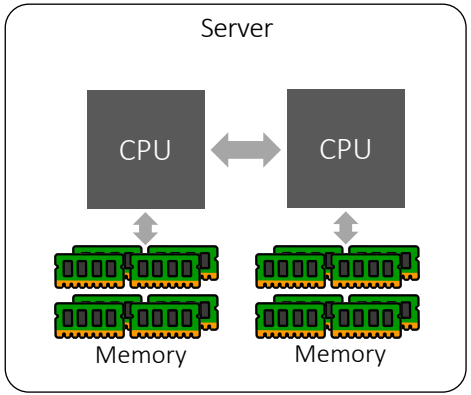
Rambus Product Revenue (~Chips)

- Robust server memory demand projected 2021 and 2022
- Strong qualification footprint and share gains on new DDR4 platforms
- Leading qualification position on DDR5 platforms
- Active ecosystem engagement on new memory architectures

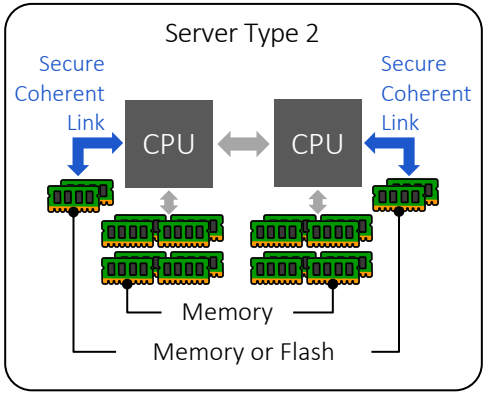


New Memory Architectures Driving TAM Expansion

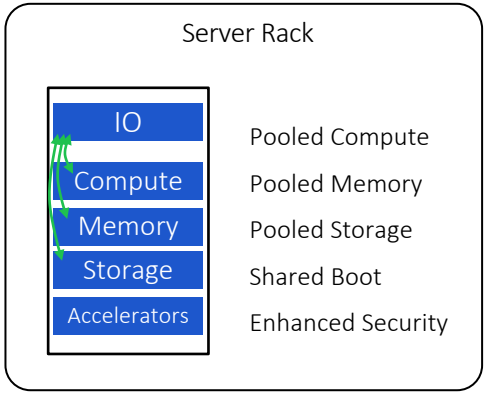
Transition to DDR5



Memory Subsystem Expansion with Serial Links (e.g., CXL)



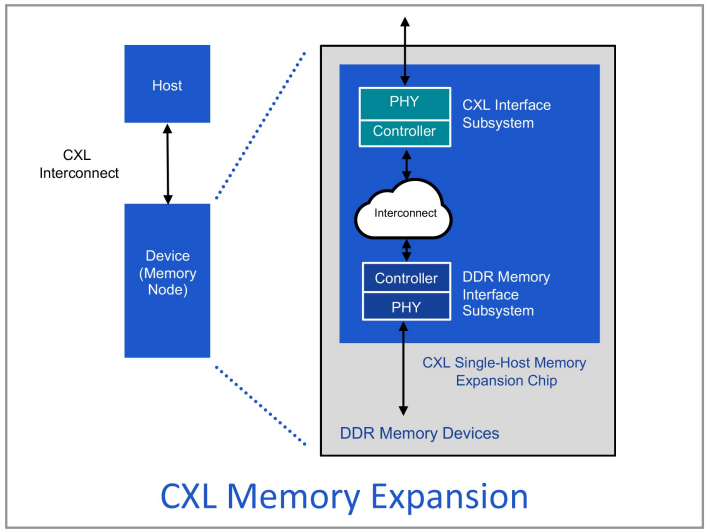
Data Center Disaggregation

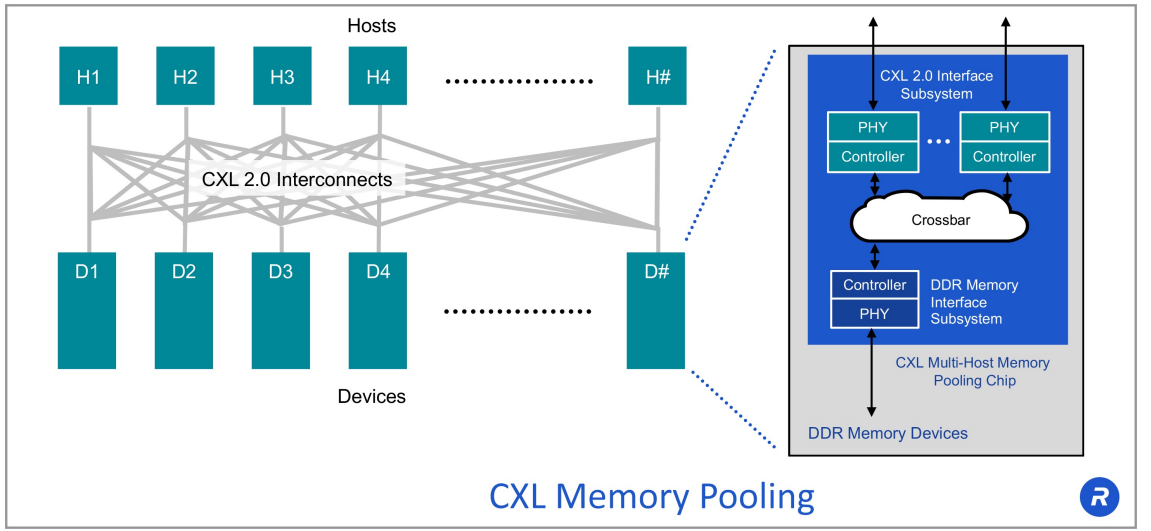


Increasing bandwidth, capacity, efficiency and security

CXL Memory Interconnect Initiative

- Establishes focused development effort on breakthrough solutions for memory expansion and pooling for advanced data center architectures
- Complements existing memory interface chip business and leverages in-house expertise in high-speed I/O, memory and security



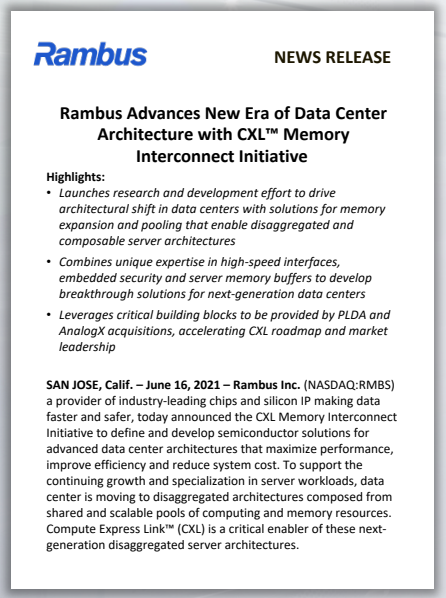


Expansion provides more main memory to Host (CPU) for higher performance on high-capacity workloads

Pooling provides additional main memory to Hosts on an "as needed" basis, improving performance, efficiency and TCO. Pooling ultimately supports disaggregation and composability.

Strategic Investments to Amplify Market Position

Announcement to ***launch*** CXL Memory Interconnect research and development



Rambus

NEWS RELEASE

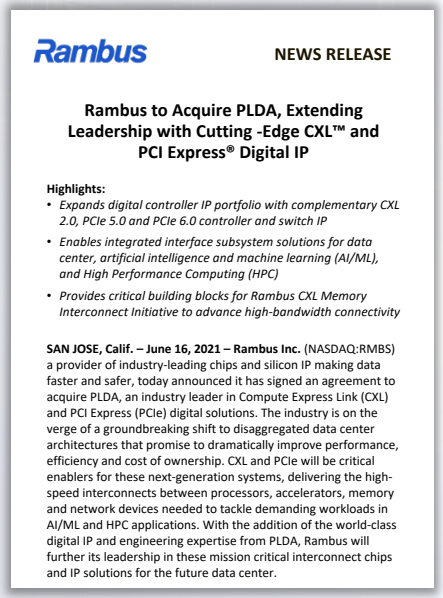
Rambus Advances New Era of Data Center Architecture with CXL™ Memory Interconnect Initiative

Highlights:

- *Launches research and development effort to drive architectural shift in data centers with solutions for memory expansion and pooling that enable disaggregated and composable server architectures*
- *Combines unique expertise in high-speed interfaces, embedded security and server memory buffers to develop breakthrough solutions for next-generation data centers*
- *Leverages critical building blocks to be provided by PLDA and AnalogX acquisitions, accelerating CXL roadmap and market leadership*

SAN JOSE, Calif. – June 16, 2021 – Rambus Inc. (NASDAQ:RMBS) a provider of industry-leading chips and silicon IP making data faster and safer, today announced the CXL Memory Interconnect Initiative to define and develop semiconductor solutions for advanced data center architectures that maximize performance, improve efficiency and reduce system cost. To support the continuing growth and specialization in server workloads, data center is moving to disaggregated architectures composed from shared and scalable pools of computing and memory resources. Compute Express Link™ (CXL) is a critical enabler of these next-generation disaggregated server architectures.

Announcement of agreement to ***acquire*** leading CXL and PCIe digital controller provider, PLDA



Rambus

NEWS RELEASE

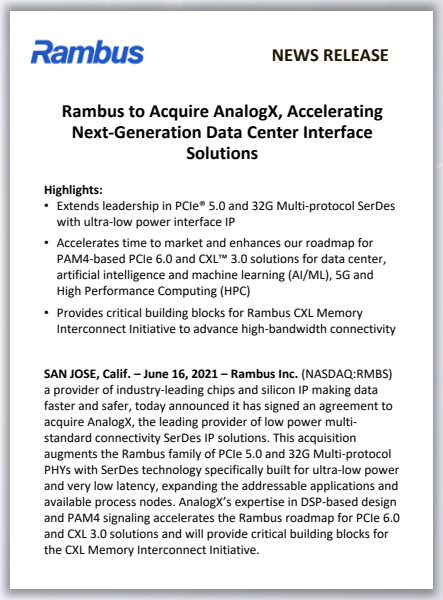
Rambus to Acquire PLDA, Extending Leadership with Cutting -Edge CXL™ and PCI Express® Digital IP

Highlights:

- *Expands digital controller IP portfolio with complementary CXL 2.0, PCIe 5.0 and PCIe 6.0 controller and switch IP*
- *Enables integrated interface subsystem solutions for data center, artificial intelligence and machine learning (AI/ML), and High Performance Computing (HPC)*
- *Provides critical building blocks for Rambus CXL Memory Interconnect Initiative to advance high-bandwidth connectivity*

SAN JOSE, Calif. – June 16, 2021 – Rambus Inc. (NASDAQ:RMBS) a provider of industry-leading chips and silicon IP making data faster and safer, today announced it has signed an agreement to acquire PLDA, an industry leader in Compute Express Link (CXL) and PCI Express (PCIe) digital solutions. The industry is on the verge of a groundbreaking shift to disaggregated data center architectures that promise to dramatically improve performance, efficiency and cost of ownership. CXL and PCIe will be critical enablers for these next-generation systems, delivering the high-speed interconnects between processors, accelerators, memory and network devices needed to tackle demanding workloads in AI/ML and HPC applications. With the addition of the world-class digital IP and engineering expertise from PLDA, Rambus will further its leadership in these mission critical interconnect chips and IP solutions for the future data center.

Announcement of agreement to ***acquire*** leading high-speed, low-power PHY provider, AnalogX



Rambus

NEWS RELEASE

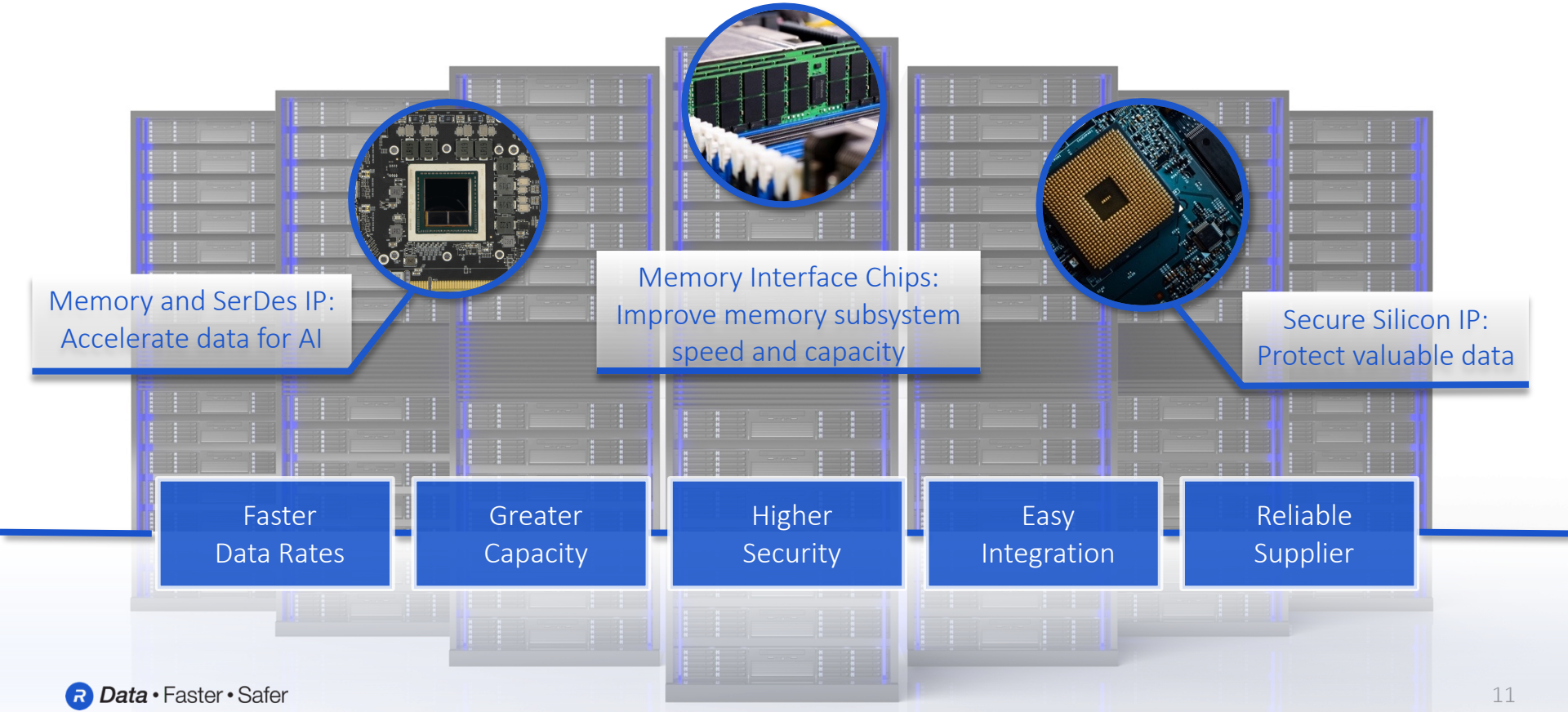
Rambus to Acquire AnalogX, Accelerating Next-Generation Data Center Interface Solutions

Highlights:

- Extends leadership in PCIe® 5.0 and 32G Multi-protocol SerDes with ultra-low power interface IP
- Accelerates time to market and enhances our roadmap for PAM4-based PCIe 6.0 and CXL™ 3.0 solutions for data center, artificial intelligence and machine learning (AI/ML), 5G and High Performance Computing (HPC)
- Provides critical building blocks for Rambus CXL Memory Interconnect Initiative to advance high-bandwidth connectivity

SAN JOSE, Calif. – June 16, 2021 – Rambus Inc. (NASDAQ:RMBS) a provider of industry-leading chips and silicon IP making data faster and safer, today announced it has signed an agreement to acquire AnalogX, the leading provider of low power multi-standard connectivity SerDes IP solutions. This acquisition augments the Rambus family of PCIe 5.0 and 32G Multi-protocol PHYs with SerDes technology specifically built for ultra-low power and very low latency, expanding the addressable applications and available process nodes. AnalogX's expertise in DSP-based design and PAM4 signaling accelerates the Rambus roadmap for PCIe 6.0 and CXL 3.0 solutions and will provide critical building blocks for the CXL Memory Interconnect Initiative.

Rambus Delivers Fast and Secure Connections for Data Center



Memory and SerDes IP: Accelerate data for AI

Memory Interface Chips: Improve memory subsystem speed and capacity

Secure Silicon IP: Protect valuable data

Faster Data Rates

Greater Capacity

Higher Security

Easy Integration

Reliable Supplier

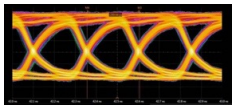
Product Leadership Driving Topline Growth

2018-2020

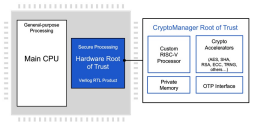
41% CAGR

Chip and Silicon IP combined revenue

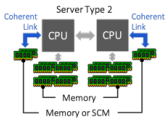
Industry's first DDR5 memory interface chips



Integrated PCIe5, HBM2E and GDDR6 memory PHY + Controller subsystems

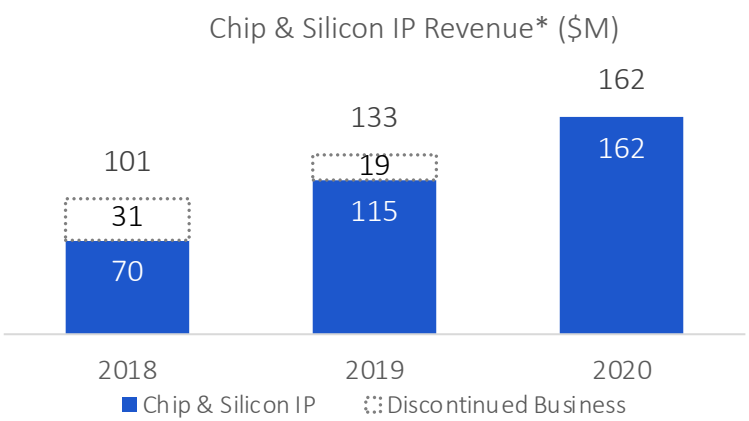


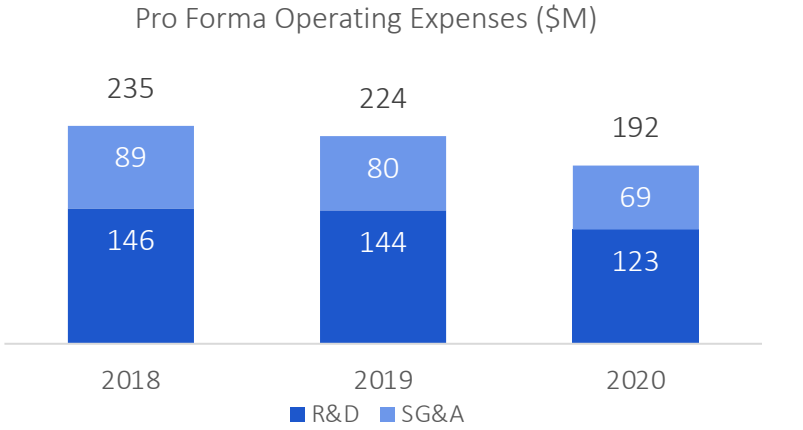
Broadest portfolio of secure root of trust, protocol engine, and crypto accelerator cores

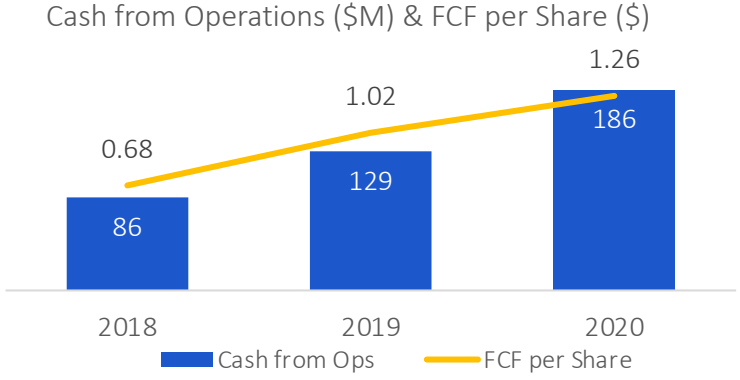


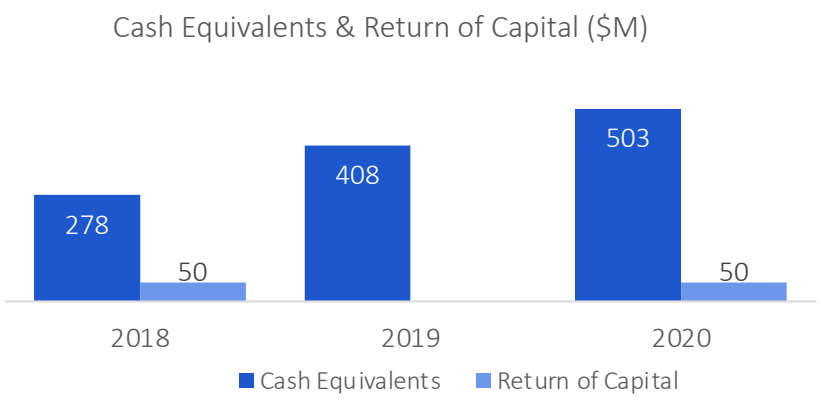
Experts in interface solutions critical for performance and utilization in emerging data center architectures

Financial Highlights









*Includes Product and Contract & Other Revenue

Rambus Investment Summary

- Amplified market opportunity in data center as memory importance increases
- Pioneer of industry-leading chips and silicon IP enabling critical performance improvements for data center and cloud
- Continued innovation feeds patent portfolio and product roadmap expansion
- Superior product execution and strong operational discipline drive solid financial results and profitable growth
- Strong cash generation enables strategic initiatives and return of capital to shareholders

Detailed Financials

Rambus
Data · Faster · Safer

Continued Strong Cash Generation

In Millions	ASC 606 Q1 2020	ASC 606 Q2 2020	ASC 606 Q3 2020	ASC 606 Q4 2020	ASC 606 Q1 2021	
Revenue	$65.8	$61.7	$56.9	$61.9	$70.4	Driven by higher Chip revenue quarter over quarter
Total Operating Costs and Expenses[1]	$63.5	$59.5	$56.7	$55.8	$58.2	Disciplined expense management through refocus on core growth initiatives
Operating Income[1]	$2.3	$2.2	$0.2	$6.1	$12.1	Operating results under ASC 606 do not reflect significant cash flows from fixed-fee licensing arrangements signed prior to the standard becoming effective
Cash from Operations	$37.3	$62.0	$44.1	$42.1	$39.5	Sustained, predictable cash generation

[1]Please refer to reconciliations of non-GAAP financial measures included in this presentation and in our earnings release

Solid Balance Sheet Supports Strategic Initiatives

In Millions	Q1 2020	Q2 2020	Q3 2020	Q4 2020	Q1 2021	
Total Cash & Marketable Securities	$435.4	$486.1	$520.2	$502.6	$529.1	Driven by continued strong cash from operations
Total Assets	$1,325.4	$1,324.1	$1,316.6	$1,251.4	$1,235.8	Strong balance sheet with limited debt $345M and $376M contract assets in Q1 2021 and Q4 2020 respectively, related to ASC 606 adoption
Stockholders' Equity	$971.6	$972.7	$965.8	$912.7	$909.4	
Cash from Operations	$37.3	$62.0	$44.1	$42.1	$39.5	Sustained, predictable cash generation

Reconciliation of Non-GAAP Financial Measures

Net Income (Loss) in Millions	Q1 2020 (ASC 606)	Q2 2020 (ASC 606)	Q3 2020 (ASC 606)	Q4 2020 (ASC 606)	Q1 2021 (ASC 606)
GAAP Net Loss	($7)	($9)	($13)	($12)	($3)
Adjustments:					
Stock-based compensation	$6	$7	$7	$6	$7
Acquisition-related/divestiture costs	$2	$2	$1	$1	$1
Amortization of acquired intangible assets	$5	$5	$5	$5	$5
Restructuring and other charges	$1	$0	$0	$3	$0
Non-cash interest expense	$2	$2	$2	$2	$2
Facility restoration costs	$0	$0	$0	$0	$0
Change in fair value of earn-out liability	($2)	$0	$0	$0	$0
Depreciation expense on unused EDA software licenses	$0	$0	$0	$2	$0
Expense on abandoned operating leases	$0	$0	$0	$0	$1
Restatement and shareholder activist costs	$0	$0	$0	$0	$3
Provision for (benefit from) income taxes	($1)	($1)	$0	($0)	($4)
Non-GAAP Net Income	**$6**	**$5**	**$2**	**$6**	**$11**

Operating Income (Loss) in Millions	Q1 2020 (ASC 606)	Q2 2020 (ASC 606)	Q3 2020 (ASC 606)	Q4 2020 (ASC 606)	Q1 2021 (ASC 606)
GAAP Operating Loss	($9)	($11)	($13)	($11)	($3)
Adjustments:					
Stock-based compensation	$6	$7	$7	$6	$7
Acquisition-related/divestiture costs	$2	$2	$1	$1	$1
Amortization of acquired intangible assets	$5	$5	$5	$5	$5
Restructuring and other charges	$1	$0	$0	$3	$0
Facility restoration costs	$0	$0	$0	$0	$0
Depreciation expense on unused EDA software licenses	$0	$0	$0	$2	$0
Expense on abandoned operating leases	$0	$0	$0	$0	$1
Change in fair value of earn-out liability	($2)	$0	$0	$0	$0
Restatement and shareholder activist costs	$0	$0	$0	$0	$3
Non-GAAP Operating Income	**$2**	**$2**	**$0**	**$6**	**$12**
Depreciation	$5	$5	$5	$7	$5
Adjusted EBITDA	**$7**	**$7**	**$5**	**$13**	**$17**

Certain amounts may be off $1.0M due to rounding.

Revenue and Licensing Billings

	ASC 606					ASC 606
In Thousands	Q1'20	Q2'20	Q3'20	Q4'20	FY 2020	Q1'21
Royalty Revenue	$21,482	$18,744	$16,602	$27,732	$84,560	$28,859
Product Revenue	$30,728	$31,725	$29,769	$21,774	$113,996	$30,781
Contract and Other Revenue	$13,567	$11,248	$10,544	$12,407	$47,766	$10,742
Total	**$65,777**	**$61,717**	**$56,915**	**$61,913**	**$246,322**	**$70,382**

In Thousands	Q1'20	Q2'20	Q3'20	Q4'20	FY 2020	Q1'21
Royalty Revenue	$21,482	$18,744	$16,602	$27,732	$84,560	$28,859
Licensing Billings[1]	$67,072	$60,687	$63,135	$64,195	$255,089	$63,506
Delta	**$45,590**	**$41,943**	**$46,533**	**$36,463**	**$170,529**	**$34,647**

In Thousands	Q1'20	Q2'20	Q3'20	Q4'20	FY 2020	Q1'21
ASC 606 Interest Income[2]	$4,437	$3,788	$3,379	$2,984	$14,588	$2,842

[1] Licensing billings is an operational metric that reflects amounts invoiced to our patent and technology licensing customers during the period, as adjusted for certain differences.

[2] Interest income associated with the significant financing component of licensing agreements as a result of the adoption of ASC 606.

GAAP to Non-GAAP Income Statement

In $ Millions	GAAP Actual Q1'21	Non-GAAP Actual Q1'21	Delta to GAAP
Revenue	$70.4	$70.4	$-
Cost of revenue	17.4	12.9	(4.4)
Research and development	32.4	28.8	(3.5)
Sales, general and administrative	23.8	16.5	(7.3)
Restructuring charges	0.4	0.0	(0.4)
Total operating cost and expenses	73.9	58.2	(15.6)
Operating income (loss)	(3.5)	12.1	15.6
Interest and other income (expense), net	0.4	2.2	1.9
Income (loss) before income taxes	(3.1)	14.4	17.5
Provision for (benefit from) income taxes	(0.5)	3.5	4.0
Net income (loss)	($2.6)	$10.9	$13.5

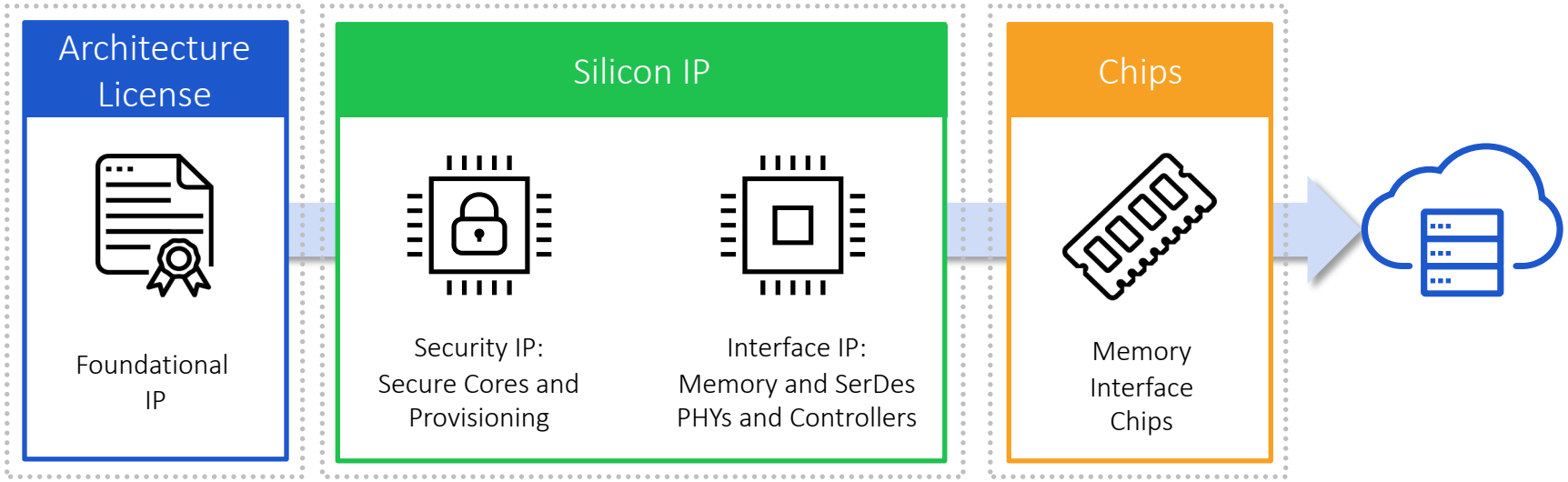
Certain amounts may be off $0.1M due to rounding.

Product Overview

Rambus

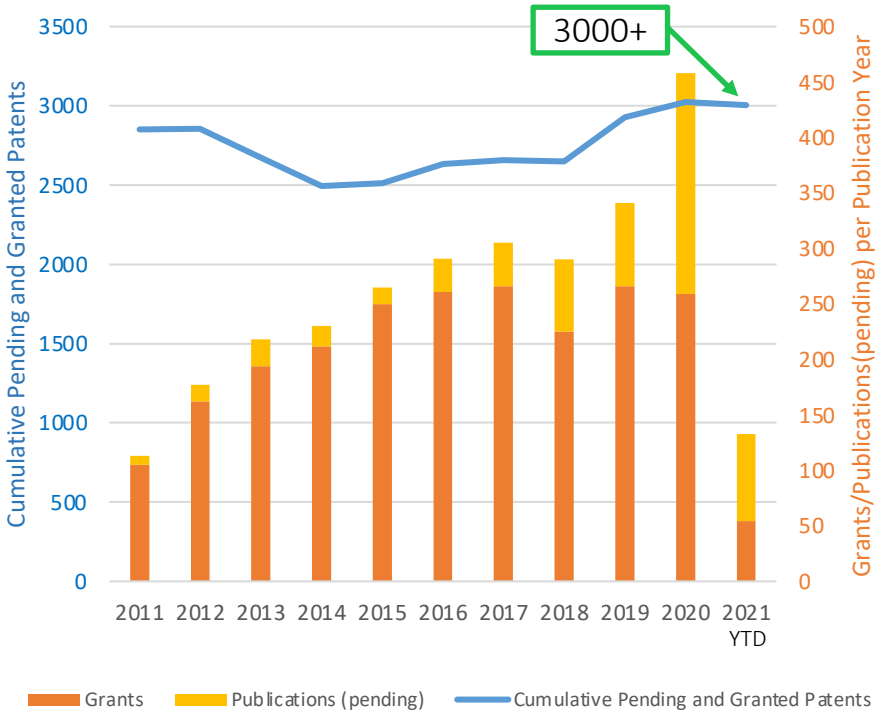
Data · Faster · Safer

Semiconductor Solutions Built on Leading-Edge IP

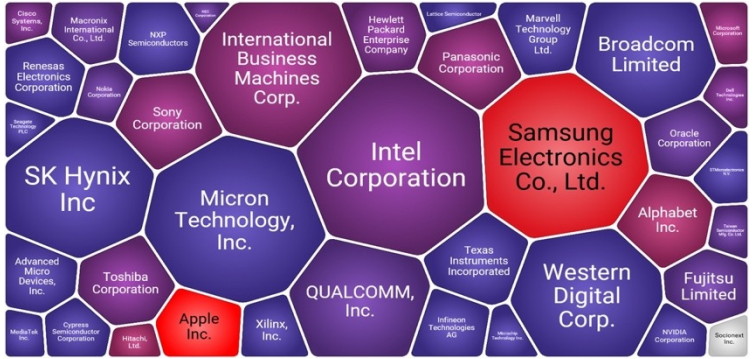


Innovating to Meet Market Needs

Growing Patent Portfolio

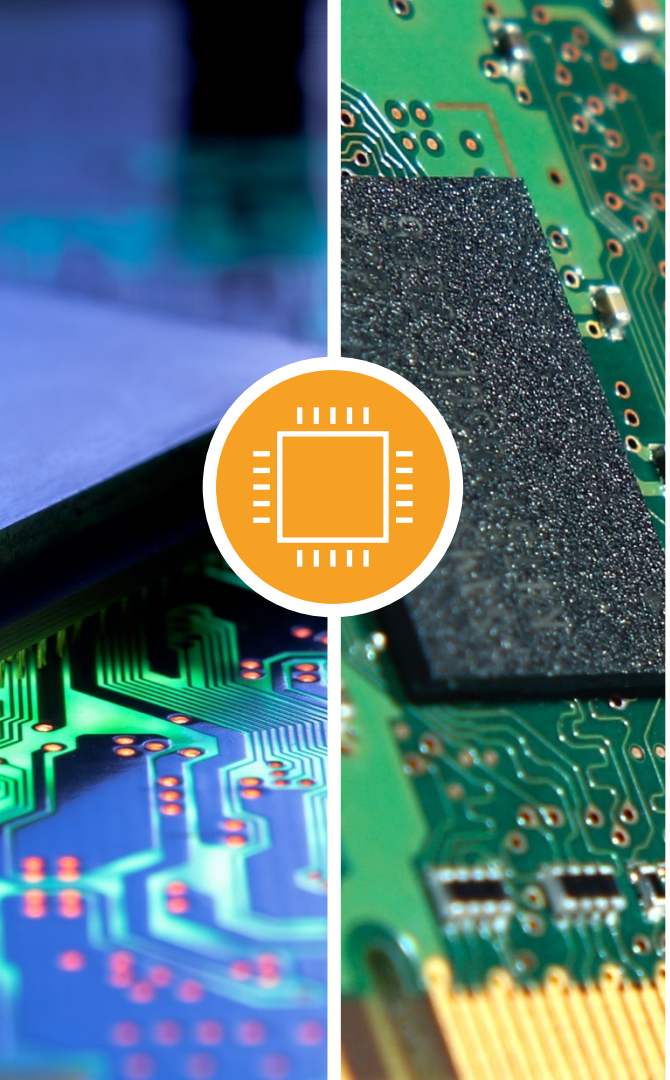


Industry Recognition of Rambus Patents



Source: Innography, patent citations

- Fundamental R&D feeds product development
- Relevant portfolio regularly cited by major industry players
- Supports predictable licensing base and sustained cash generation

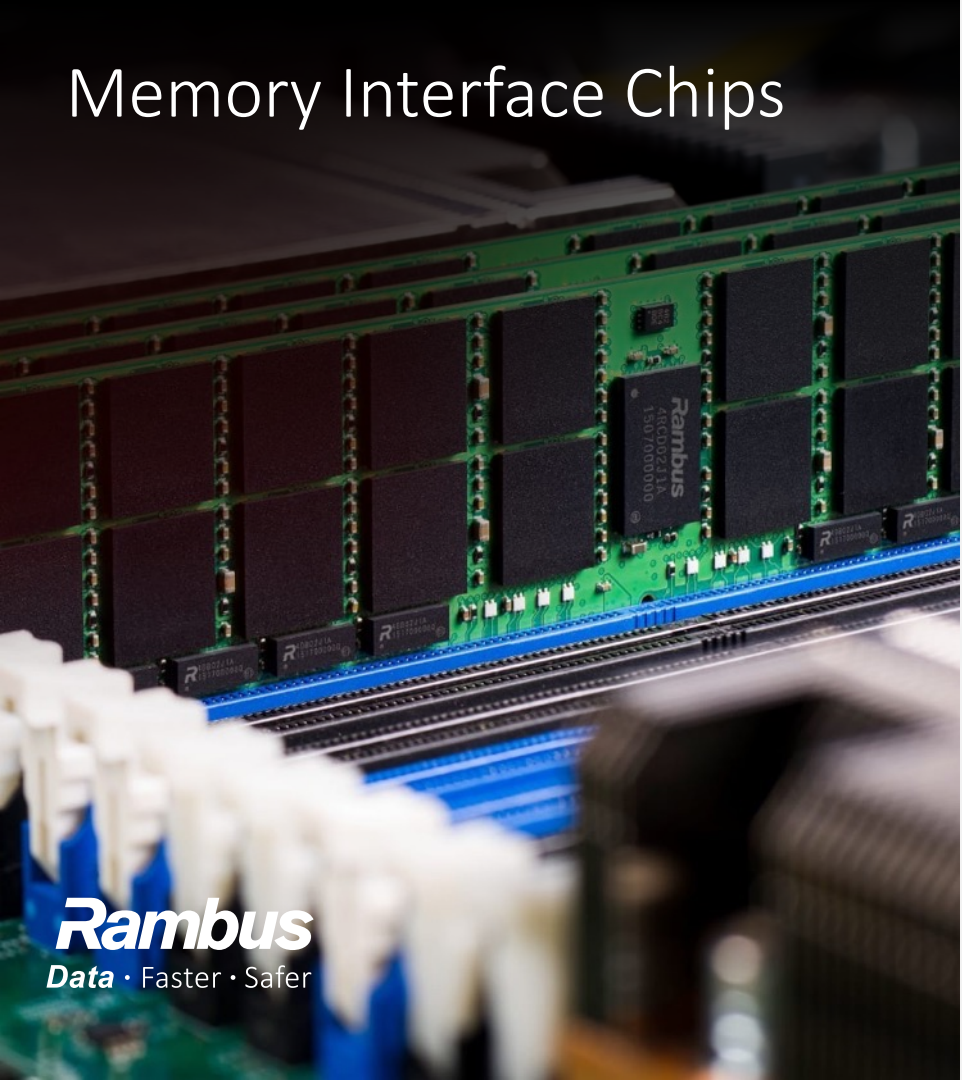


Memory Interface Chips

Rambus

Data · Faster · Safer

Memory Interface Chips



Built for speed, power efficiency and reliability, the DDRn memory interface chips for RDIMM, LRDIMM and NVDIMM server modules deliver top-of-the-line performance and the capacity needed to meet the growing demands on enterprise and data center systems.

Industry-leading Performance

- Fully-compliant with the latest JEDEC standards
- Operational speeds up to 4800 Mbps

Enhanced Margin

- Wide margin I/O design with advanced programmability
- Exceed JEDEC reliability standards for ESD and EOS

Optimized Power

- Advanced power management
- Frequency-based, low-power optimization

Superior Debug and Serviceability

- Integrated tools for bring-up and debug
- Works out-of-the-box with no BIOS changes required

Memory Interface Chips

Enabling performance and capacity in server DIMMs

DDR5
DB & RCD

- Per JEDEC Direction
- Speeds of 4800 Mbps
- Ongoing qualifications

AVAILABLE IN PRODUCTION

DDR4
DB & RCD

- JEDEC Compliant
- Speeds up to 3200 Mbps
- Multiple OEM qualifications

AVAILABLE IN PRODUCTION

NV
DDR4 NVRCD

- JEDEC Compliant
- Speeds up to 3200 Mbps
- Ongoing qualifications

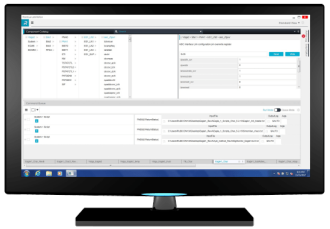
AVAILABLE IN PRODUCTION

DDR3
DB & RCD

- JEDEC Compliant
- Speeds up to 2133 Mbps
- Multiple OEM qualifications

AVAILABLE IN PRODUCTION

Smart tools for easy integration and reduced time to market



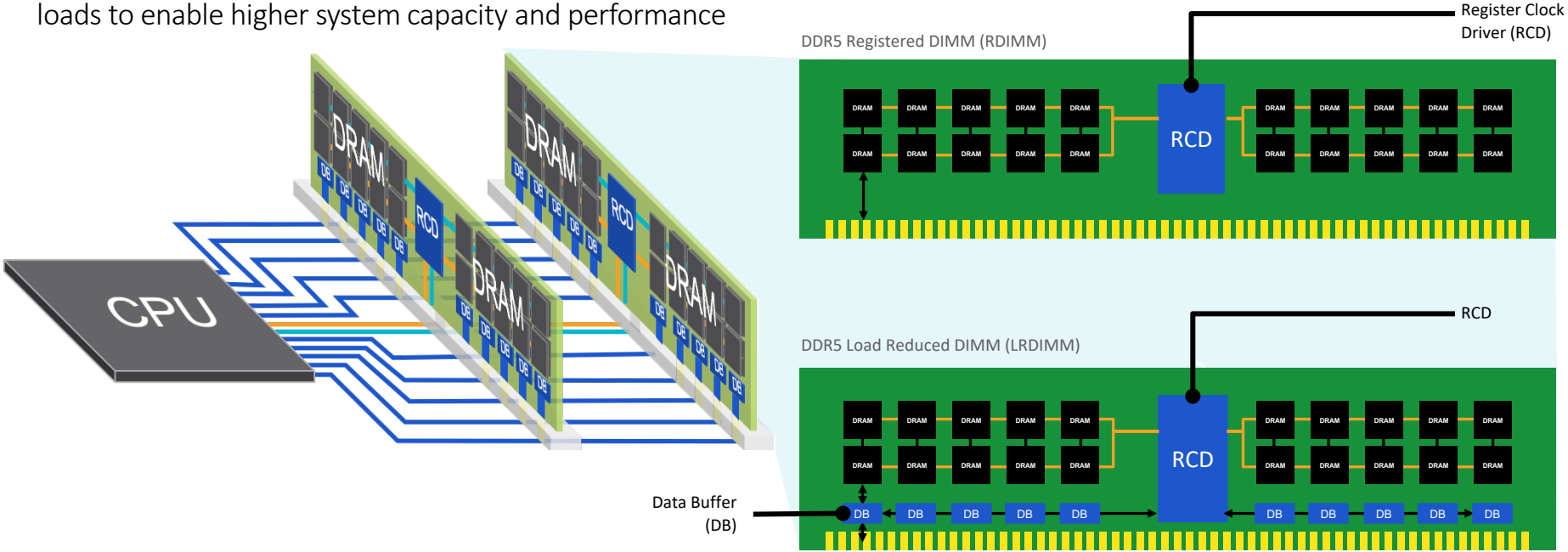
LabStation Platform
and Buffer BIOS Integration Tool

Validated solutions with partners

SAMSUNG SK hynix Micron

DDR DIMMs Boost Capacity and Bandwidth

DIMM Memory Interface chips reduce the number of loads to enable higher system capacity and performance



Memory Interface Chips = RCD + DB

Silicon IP

Rambus

Data · Faster · Safer

Silicon IP: Memory & SerDes PHYs and Controllers

Rambus
Data · Faster · Safer

Across a broad spectrum of applications spanning automotive, artificial intelligence (AI), Internet of Things (IoT), network edge, and data center, there is a common need to move more data faster. Rambus memory and SerDes IP deliver the performance needed by the most demanding applications to move the data at blinding fast speeds.

HBM2E Memory Subsystem

- Fully-integrate and silicon-proven PHY and controller
- Running at industry's fastest data rate up to 4.0 Gbps
- Ideal for AI/ML training, graphics and networking applications

GDDR6 Memory Subsystem

- Fully-integrate and silicon-proven PHY and controller
- Running at industry's fastest data rate up to 18.0 Gbps
- Ideal for AI/ML interference, automotive, graphics and networking applications

PCIe 5

- Co-validated PHY and controller
- PHY supports Compute Express Link (CXL)
- Multiple configurations to support broad range of applications

Memory Interface Solutions

Memory PHY and digital controller solutions

HBM2E
7nm & 14/11nm

- 3.6 Gbps
- 1024-bit
- 2.5D design architecture

Si

GDDR6
7nm

- 12-18 Gbps
- 2x 16-bit channels

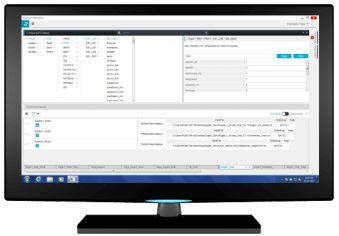
Si

DDR4/3
12nm & 28nm

- 3200 Mbps
- x16 to x72-bits
- 1-4 Ranks
- DFI 4.0

Si

Integrated tools for easy bring-up and characterization



LabStation Platform

- Easy-to-use PC Interface
- Interface to 3rd party software
- Pre-defined test scripts
- PHY control settings
- External instrument control
- System characteristics and analysis

Verification tools

avery design systems

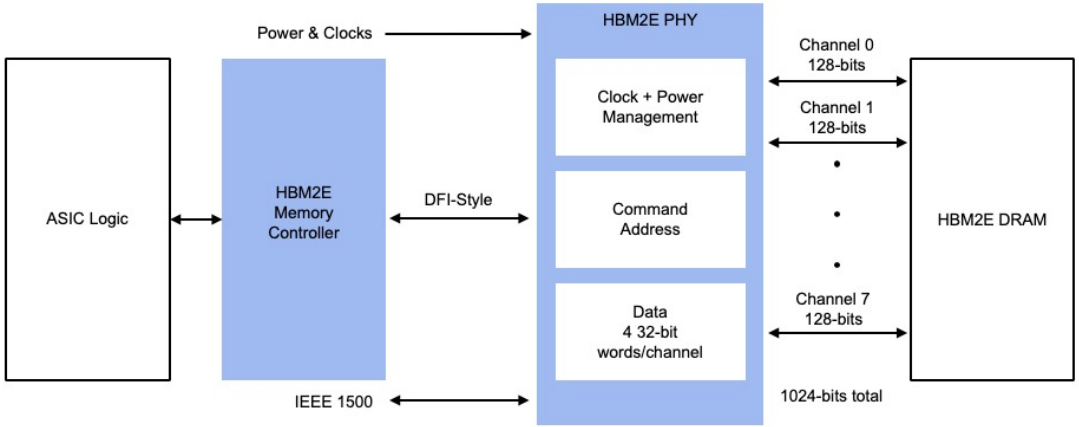
Complete HBM2E Interface

Applications

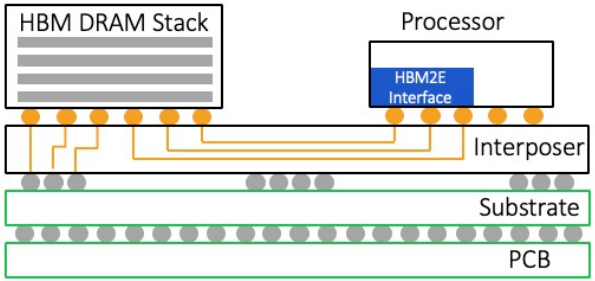
- AI/ML
- Graphics
- Networking

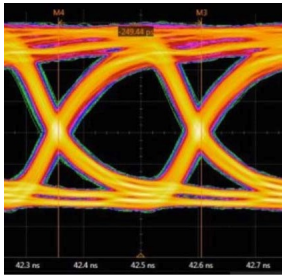
Features

- JEDEC standard compliant
- 7nm process node
- 461 GB/s maximum bandwidth
- Speed bins to 3.6 Gbps with operation to 4.0 Gbps
- Support for stacks of 2, 4, 8 or 12 DRAM



HBM2E Memory Interface Subsystem
(Controller & PHY)





World's fastest HBM2E Operating at 4.0 Gbps

Complete GDDR6 Interface

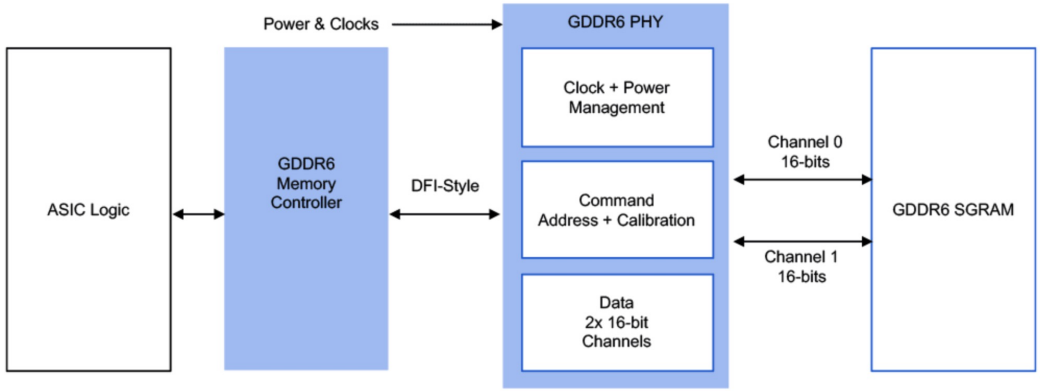
Applications:

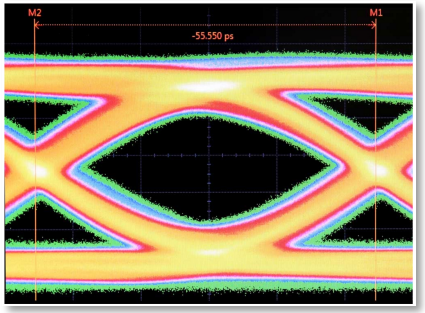
- AI/ML
- Automotive
- Graphics
- Networking

Features:

- JEDEC standard compliant
- 7nm process node
- 72 GB/s maximum bandwidth
- Speed Bins: 12, 14, 16, 18 Gbps
- Supported DRAM: 8, 12, 16 Gbit
- ASIC Interface: DFI style
- Supports clam shell mode
- All training and calibration modes support

GDDR6 Memory Interface Subsystem
(Controller + PHY)





GDDR6 18 Gbps Transmit Eye

High-Speed SerDes Solutions

SerDes PHY and digital controller solutions

PCIe 5
7nm

- PCIe 5
- CXL (PHY)
- PCIe 4/3/2

Si

32G
12nm & 22nm

- CEI-28/25/11
- 40/10GbE
- JESD204B/C
- CPRI

Si

28G
12nm

- CEI-28/25/11
- 40/10GbE
- FC28
- XFI/XAUI

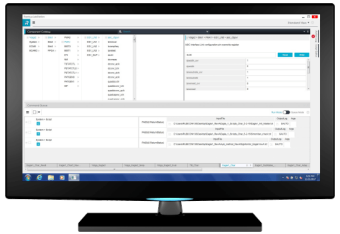
Si

16G
12nm & 28nm

- PCIe 4/3/2
- CEI 11/6
- XFI/XAUI
- SATA
- SAS

Si

Integrated tools for easy bring-up and characterization



LabStation Platform

- Easy-to-use PC Interface
- Interface to 3rd party software
- Pre-defined test scripts
- PHY control settings
- External instrument control
- System characteristics and analysis

Verification tools

avery design systems

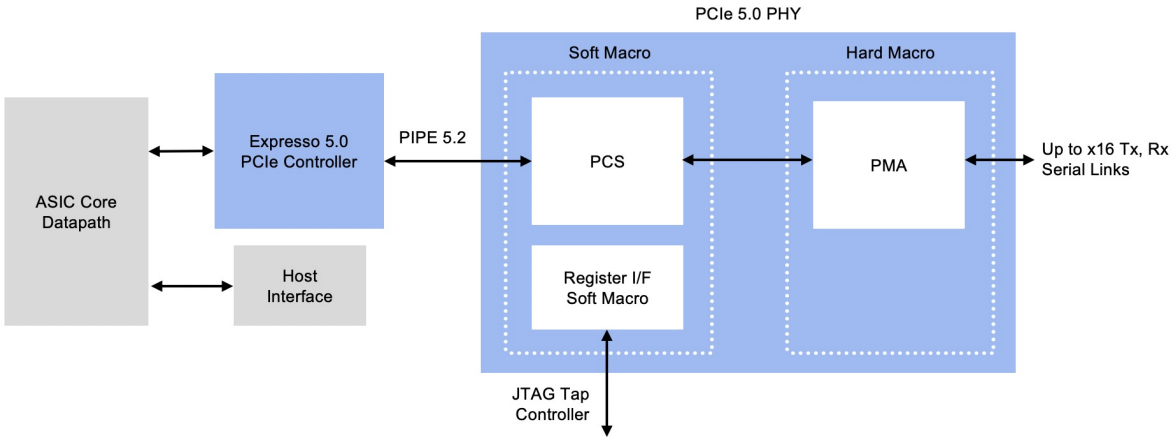
Complete PCIe 5.0 Interface

Co-validated PCIe 5 PHY and Controller

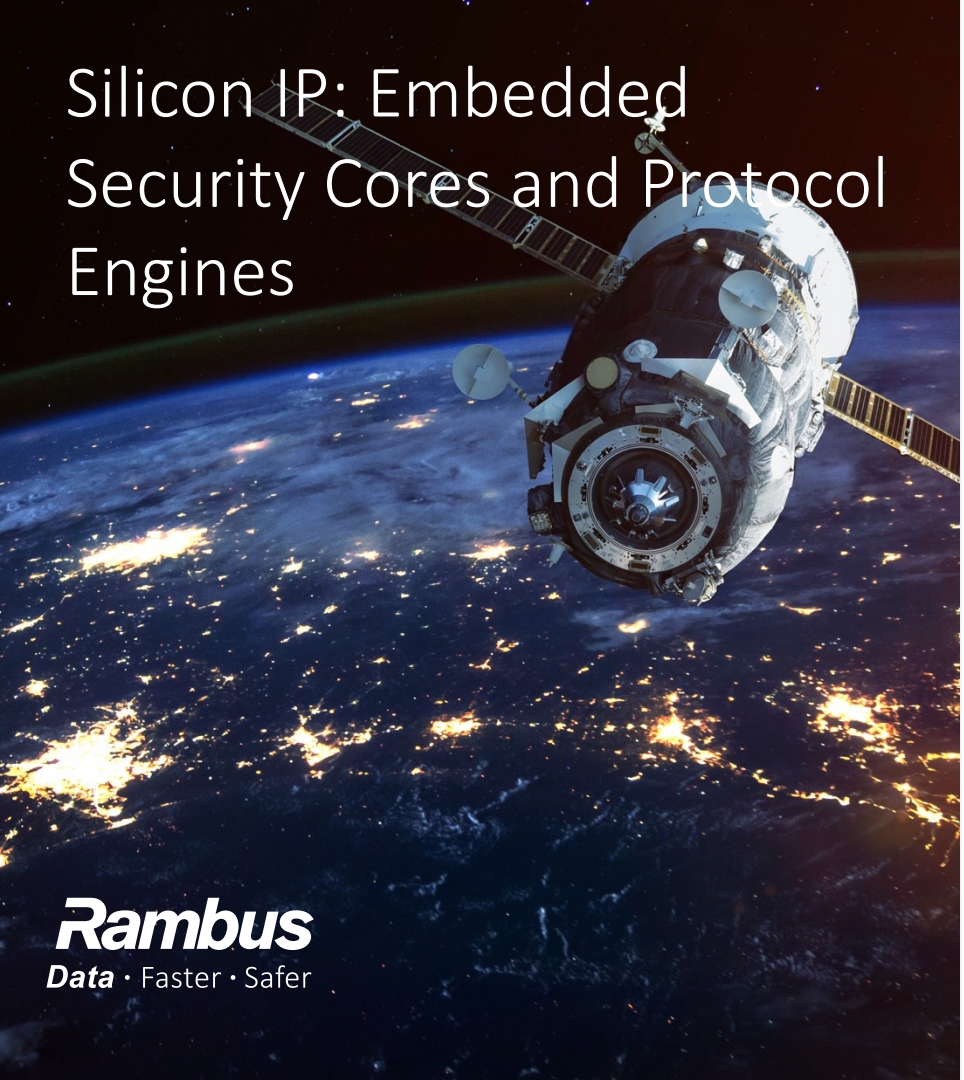
- Eases SoC integration effort
- Reduces design risk
- Speeds time to market

Features

- Backward compatible to PCIe 4/3/2
- PHY supports Compute Express Link (CXL)
- X1, X2, X4, X8 and X16 lane configuration support
- Supports >36dB of channel insertion loss
- Available in 7nm



PCIe 5 Interface Subsystem



Silicon IP: Embedded Security Cores and Protocol Engines

Rambus secure silicon IP helps protects data at rest and in motion across a broad range of applications and throughout a device's lifecycle. Securing electronic systems at their hardware foundation, our embedded security solutions span areas including root of trust, tamper resistance, content protection and trusted provisioning.

Root of Trust Cores

- Portfolio of solutions from fully-programmable secure co-processors to highly-compact state machines
- Provides hardware-based foundation for security
- Optimized for broad range of applications including AI/ML, automotive, IoT and defense

800G MACSec Engine

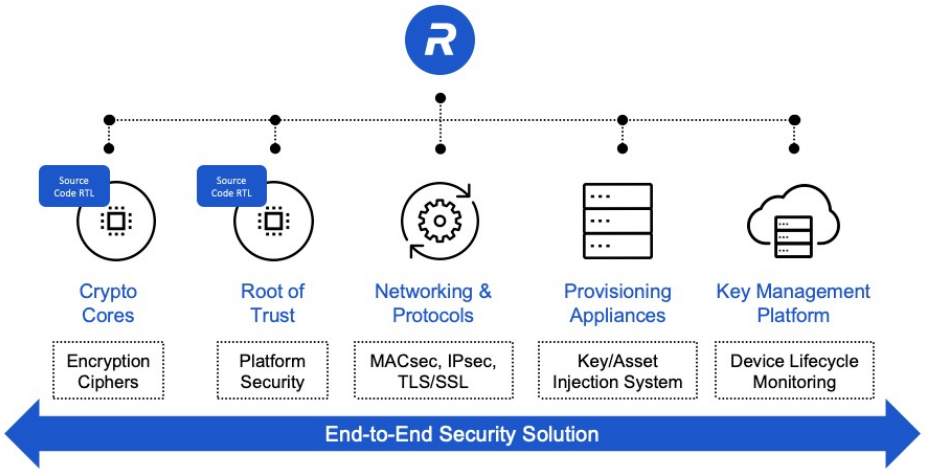
- Protects data in motion with robust Layer 2 security anchored in hardware
- Operates at full line-rate up to 800 Gbps supporting real-time applications
- Offers easy integration into networking SoCs and ASICs

Provisioning and Key Management

- Provision cryptographic information securely in untrusted environments
- Protect against cloning, reverse engineering, and counterfeiting
- Manufacturers can leverage securely provisioned keys and identities to enable supply chain integrity.

Silicon IP: Security

Protecting semiconductors and their secrets from design and manufacturing through deployment and end-of-life



Secure Cores

Root of Trust | Protocol Engines | Crypto Cores | Anti-Counterfeiting

Secure Protocols

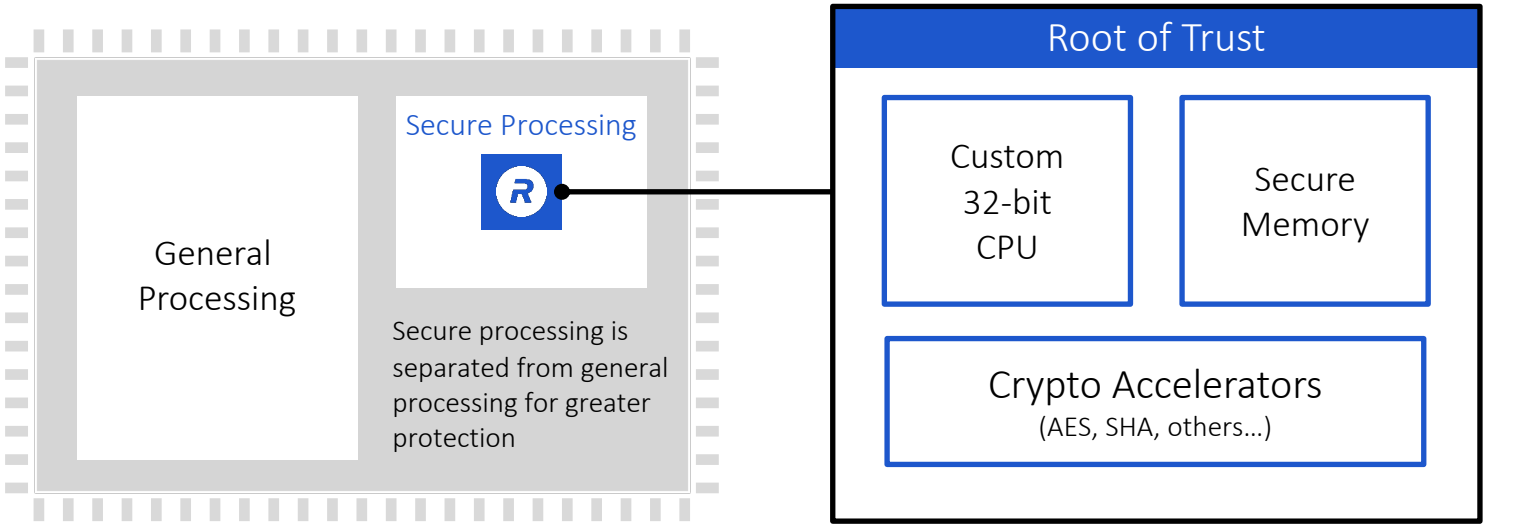
Secure Provisioning

Key and Data Injection | Device Key Management

Root of Trust

Portfolio of solutions from fully-programmable secure co-processors to highly compact state machines

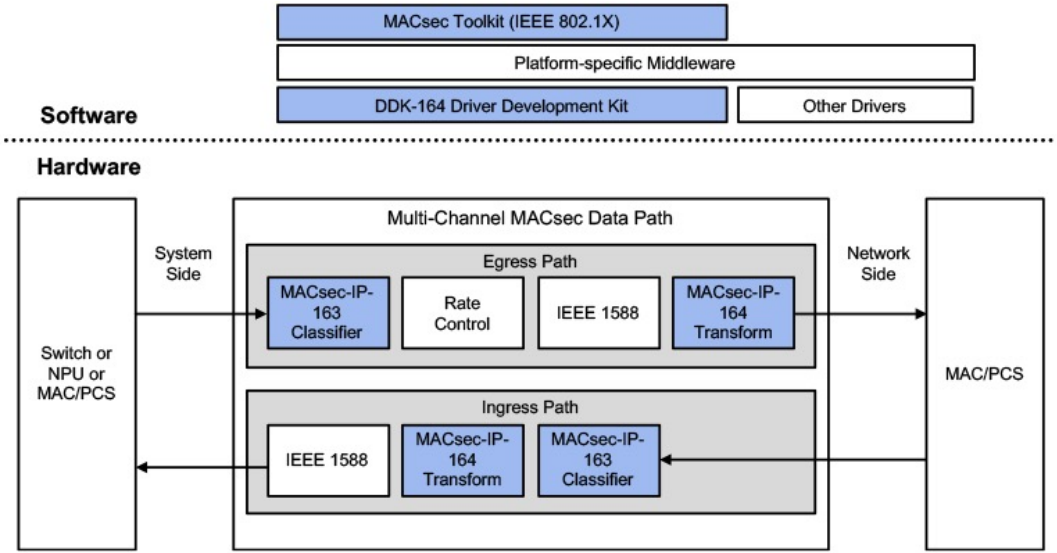
- Provides hardware-based foundation for security
- Offers wide range of cryptographic functions and anti-tamper protections



Secure Co-Processor Root of Trust (RT-600 Series)

800G MACsec Protocol Engine

- Protects data in motion with robust Layer 2 security anchored in hardware
- Operates at full line-rate up to 800 Gbps supporting real-time applications
- Offers easy integration into networking SoCs and ASICs



Multi-channel Protocol Engine Supports 100G to 800G MACsec

Thank you

Rambus

Data · Faster · Safer